Ph. D. DISSERTATION

Solution-processed high-*k* dielectrics for organic/inorganic thin-film transistors and CMOS circuit applications

용액 공정 고유전상수 절연체를 이용한
유무기 박막트랜지스터 및 상보형 회로
응용에 대한 연구

BY

SEON-BEOM JI

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DEPARTMENT OF ELECTRICAL ENGINEERING AND
COMPUTUER SCIENCE
COLLEGE OF ENGINEERING
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지도교수 홍 용 택

이 논문을 공학박사 학위논문으로 제출함

2015 년 2 월

서울대학교 대학원

전기컴퓨터 공학부

지 선 범

지선범의 공학박사 학위논문을 인준함

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위 원 장 : 이 종 호 (인)

부위원장 : 홍 용 택 (인)

위 원 : 이 창 희 (인)

위 원 : 박 성 규 (인)

위 원 : 김 영 훈 (인)

Abstract

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Zinc-oxide (ZnO)-based materials have been widely investigated as an active channel layer of thin-film transistors (TFTs) due to their high mobility and optically high transparency related with the wide band gap and application to solution-process. Many kinds of ZnO-based TFTs have been reported for backplanes of active matrix liquid crystal displays (AMLCDs) and active matrix organic light emitting diodes (AMOLEDs). However, even though ZnO-based materials can be fabricated by solution-based processes, which are expected to simple and low cost method, most

devices have been fabricated by expensive vacuum processes such as pulsed laser deposition (PLD) and sputtering method. Recently, there are many efforts for reducing the operational voltage of TFTs using high capacitance dielectrics. By incorporating the high capacitance dielectrics, more charges can be accumulated at dielectric and semiconductor interfaces at the same bias condition, hence, TFTs and circuits can be operated under a low voltage condition. Additionally, low-power consumption and high electrical performance including a low subthreshold swing (S.S) can be achieved.

In this dissertation, oxide TFTs and high-*k* dielectrics fabricated by solution-process are studied for low voltage high-performance TFTs and all solution-processed organic/inorganic hybrid complementary metal-oxide-semiconductor (CMOS)-type circuit applications.

First, the solution-processed indium-gallium-zinc-oxide (IGZO) TFTs, composed of inkjet-printed active channel layer and Ag source/drain (S/D) electrodes, were demonstrated. Inkjet-printed IGZO TFTs exhibited the high mobility above 2 cm^2/Vs at 400 ^oC annealing temperature. Optimizations of inkjet-printing and thermal annealing conditions were required to achieve high performance characteristics.

Second, high-*k* Al_2O_3 and ZrO_2 gate dielectrics were fabricated by spin-coating method for improving the electrical performance and reducing the operating voltage of oxide and organic TFTs. High capacitance of gate dielectrics enabled oxide and organic TFTs to operate in low-voltage condition under the 5 V. In particular, Al_2O_3 dielectric exhibited the amorphous phase and better TFT electrical behaviors such as

high mobility and steep S.S. than ZrO_2 dielectrics in both organic and oxide TFTs. And all solution-processed high-performance low-voltage IGZO TFTs were demonstrated. Additionally, a metal-insulator-semiconductor-metal (MISM) capacitor measurement was proposed for accuracy estimation of parameters due to the possibility of the additional electric double layer (EDL) formation through the mobile ions migration.

Finally, an organic/inorganic hybrid structure approach was proposed to achieve CMOS-type inverters. Demonstrated organic/inorganic hybrid CMOS-type inverter structure showed the improved electrical performance compared to previous reported inverters composed of only p-type TFTs. The effect of high-*k* dielectric on the hybrid CMOS-type inverter was also investigated to enhance the inverter performance.

Keywords: thin-film transistors (TFTs), indium-gallium-zinc-oxide (IGZO), oxide semiconductor, high-*k* dielectrics, complementary metal-oxide-semiconductor (CMOS), inverter, solution-process, inkjet-printing, spin-coating, pentacene, organic semiconductor

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Contents

List of Figures

List of Tables

Chapter 1 Introduction

1.1 Oxide Semiconductor Thin-Film Transistors

Flat panel display (FPD) technologies have been extensively developed over the several decades for manufacturing the large scale size, thin, high resolution, and multi-functionality embedded display such as televisions, monitors, and smartphones. Various types of FPDs have been reported and commercialized such as plasma display panels (PDPs), active matrix liquid crystal displays (AMLCDs), electronic papers, and active-matrix organic light emitting diodes (AMOLEDs) [1-4]. In particular, among the FPDs, AMLCDs have been successfully commercialized in display market over the past decade due to the huge infrastructure and the cost effective manufacture. Also, non-emissive AMLCDs have the advantages of large scale, light, thin, high resolution and low manufacturing cost. However, the slow response of the LC and the narrow viewing angle are the current issues of the AMLCD technology. In addition, the high mobility semiconductors are required to operating the large and high resolution display with high frame rates. On the contrary, emissive AMOLEDs have the merits of light, thin, high resolution, fast response, and wide viewing angle. However, AMOLEDs require the high mobility

thin-film transistors (TFTs) for the current driving of OLED devices as well as the switching. Besides, electrically and environmentally stable TFTs are required to the use of driving TFTs in OLEDs because the small degradation of a threshold voltage in TFTs lead to the mura, which is the brightness differences between pixels.

A hydrogenated amorphous silicon (a-Si:H) have been used in FPDs as the active channel layer of TFTs [5-6]. a-Si TFT technologies have the merits in uniformity, but the low mobility of a-Si (~ 0.5 cm^2/Vs) limits the increase of display resolution as well as the use of driving TFTs of AMOLEDs. Various semiconductor materials including Si-based materials, organic materials, and oxide semiconductors have been investigated to alternate the a-Si:H TFTs. Low-temperature polycrystalline silicon (LTPS) TFTs have been widely investigated to the candidate material of a-Si due to the high mobility of over 30 cm^2/Vs, the good stability against light and electrical stresses, the potential of circuit integration. However, LTPS TFTs have the problems of non-uniformity related with the grain boundaries during the crystallization and complicated cost high fabrication processes [7-8]. Recently, amorphous oxide semiconductors (AOSs) are the candidate material of TFTs to solve the drawback of a-Si:H TFTs and LTPS TFTs [9-13]. AOSs, which composed of post-transition heavy metal cations, show the high mobility (> 10 cm^2/Vs). It is resulted from the formation of band conduction carrier transport unlike covalent semiconductors. Moreover, AOSs exhibit the good uniformity, high transparency in visible region, circuit integration, solution-processing, and process compatibility of a-Si:H TFTs. Thus, AOSs have been rigorously researched to achieve large scale and high resolution AMLCDs and AMOLEDs as well as transparent displays as

shown in Figure 1.1 [14]. Furthermore, the manufacturing cost can be reduced by utilizing the solution-processes such as spin-coating and printing for deposition of AOSs as well as embedding the gate driver circuits and other electronic circuits on the display panel. Properties of a-Si:H, LTPS, and AOS TFTs are summarized in Table 1.1.

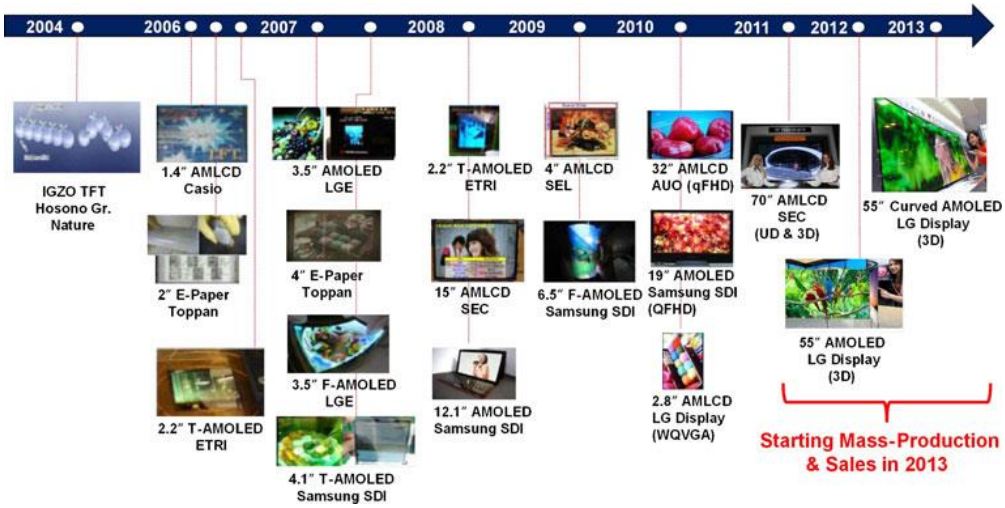


Figure 1.1 Overview of oxide semiconductor-based display technology developments (ref. [14])

Table 1.1 Properties of a-Si:H, LTPS, and AOS TFTs (ref. [14])

	a-Si:H TFT	LTPS TFT	AOS TFT
Mobility (cm^2/Vs)	0.5	> 30	1 ~ 20
Uniformity	Good	Poor	Good
Polarity	n-ch	CMOS	n-ch
Cost	Low	High	Low
Yield	High	Low	High
Vth Shift	> 10 V	< 0.5 V	< 1 V
Light stability	Poor	Good	Medium
Circuit integration	No	Yes	Yes

1.2 Solution-Process, CMOS, and High-*k* Dielectrics

Solution-based processes, which mean the fabrication method for the deposition employing the precursor type or nanoparticle type of material solutions including metals, semiconductors, and dielectrics, have been extensively studied for the electronic devices as illustrated in Figure 1.2 [14-15]. Various methods such as spin-coating [16], inkjet-printing [17], roll-to-roll [18], drop-casting, gravure-coating [19], and screen-printing [20] have been used for the solution-based processes as shown in Figure 1.3. Solution-processing has the advantages of simple, low cost, and potential of applicable to large area substrate. In particular, inkjet-printing has the merits of maslkess patterning due to direct pattern definition, non-vacuum process, large area manufacturing, high throughput and economical use of the inks. In comparison to conventional vacuum processes, inkjet-printing process can replace the 64 % of the conventional microelectronic process cost as shown in Figure 1.4 [21]. Also, the increase of demand for printed electronics including organics and inorganics is expected as shown in Figure 1.5 [22].

From a designing of circuit perspective, a complementary metal-oxide-semiconductor (CMOS) is required due the low-power consumption and simple circuit design [22]. However, AOSs typically show the n-type behavior, thus it is hard to fabricate the CMOS circuits using AOSs. Hence, approaches of combination of organic and oxide semiconductors are required.

Recently, demands on low power consumption portable electronic devices have accelerated the use of high dielectric constant (high-*k*) materials to the gate insulator of TFTs [23]. High-*k* dielectrics can induce more charges at

dielectric/semiconductor interface at the same gate bias compared to SiO_2 dielectric, TFTs and circuits can be operated in low-voltage condition and eventually power consumption can be reduced as shown in Figure 1.6.

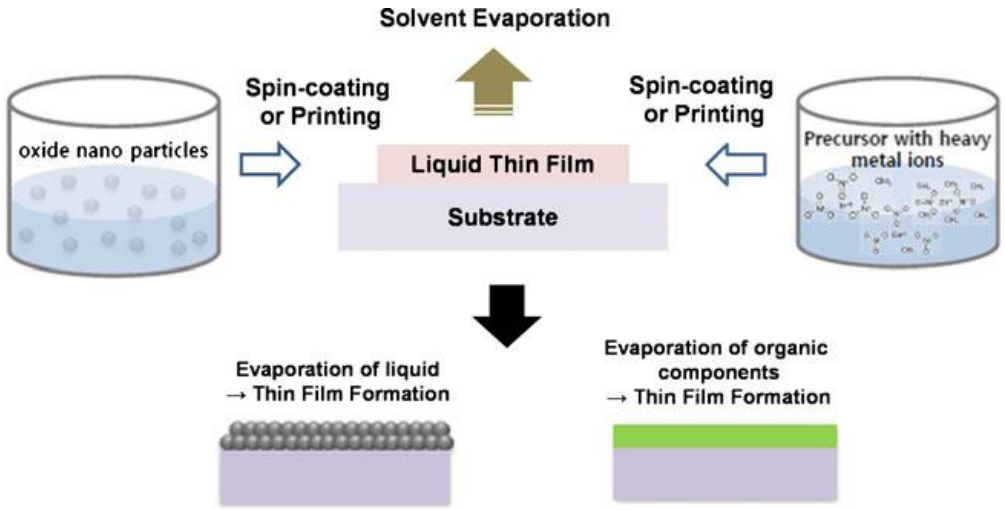


Figure 1.2 A process of film deposition using solution-based method from nanoparticle type and precursor type solution (ref. [14]).

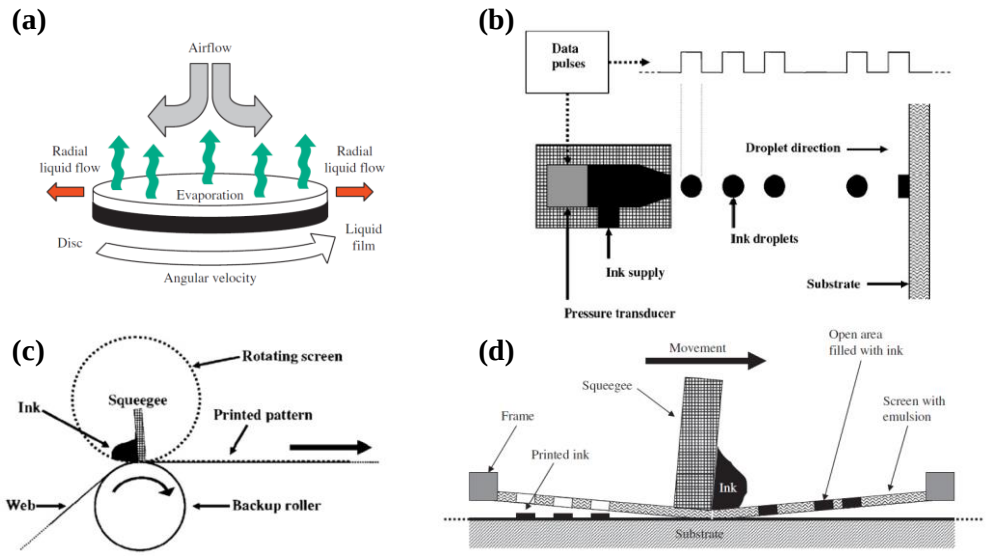
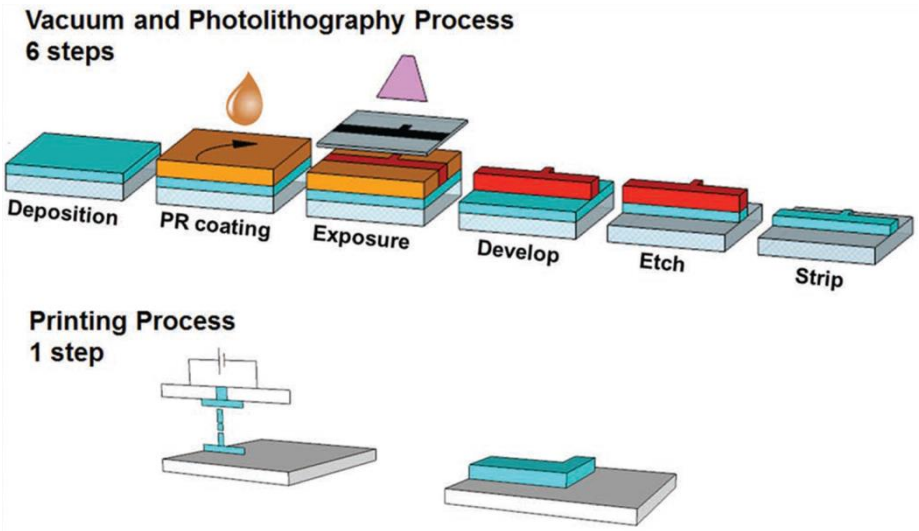
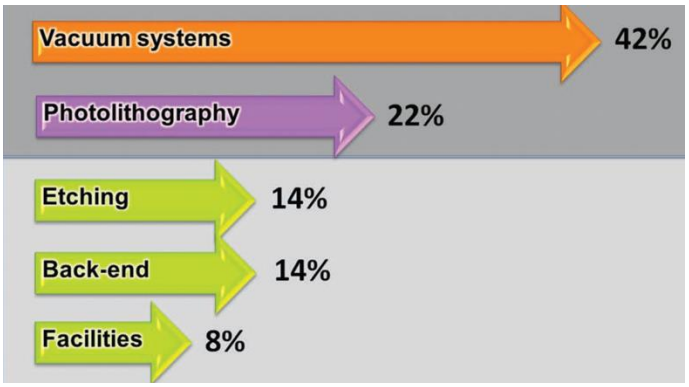


Figure 1.3 Various deposition techniques of solution-process: (a) spin-coating, (b) piezoelectric type inkjet-printing, (c) roll-to-roll and (d) screen printing (ref: [15]).



(a)



(b)

Figure 1.4 (a) Comparison of conventional vacuum process and printing process for thin-film deposition and patterning. (b) Normalized costs related to each process step in vacuum process (ref: [21]).

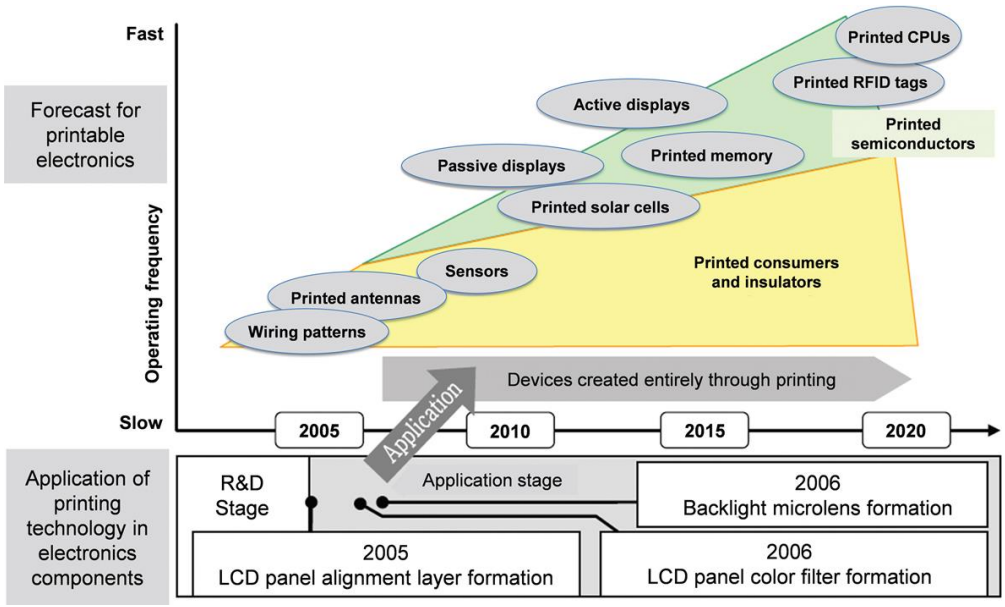


Figure 1.5 Forecast for printable electronics and application of printing technology in electronics components (ref: [22]).

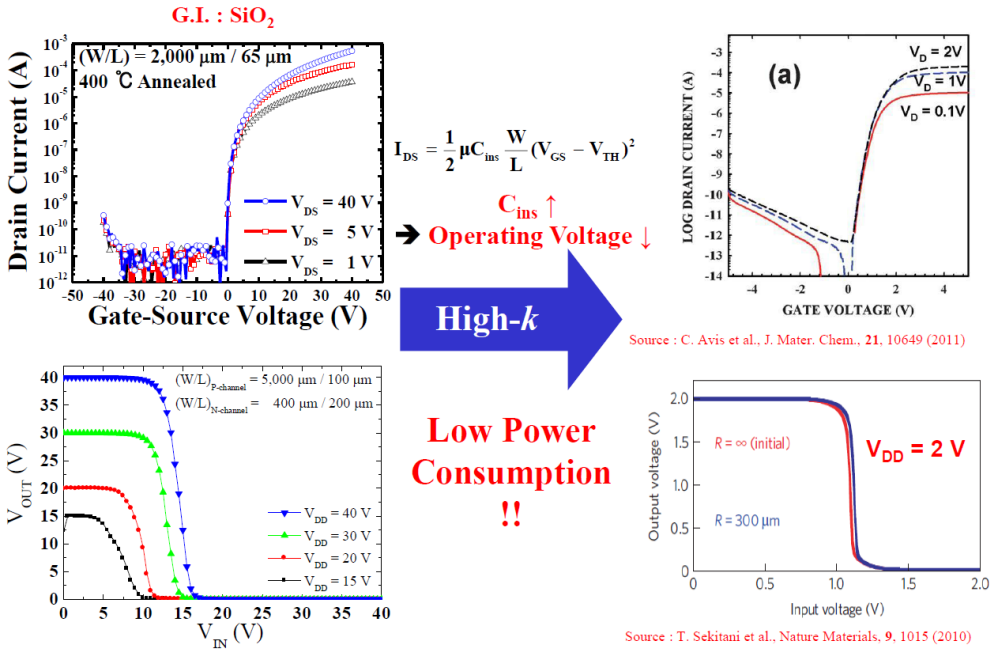


Figure 1.6 Expected results employing the high-*k* dielectrics.

1.3 Organization of This Dissertation

This dissertation introduces the studies on the solution-processed high-*k* dielectrics for low-voltage TFTs and organic/inorganic hybrid CMOS-type circuit applications. N-type and p-type semiconductors, S/D electrodes, and high-*k* dielectrics were fabricated by solution-process methods. Al_2O_3 and ZrO_2 layers were investigated to improve the electrical characteristics of both n-type and p-type TFTs for CMOS applications. And dielectric dispersion behavior of Al_2O_3 layer and their effect on the IGZO TFT characteristics were studied.

Chapter 1 includes a brief history of recent flat panel display technology with various TFTs. And advantages of solution-process, approach to CMOS-type circuit, and demand for high-*k* dielectrics are introduced.

Chapter 2 introduces the solution-processed IGZO TFTs with both active channel layer and Ag S/D electrodes were inkjet-printed. Optimization of inkjet-printing, characterization of IGZO precursor solution and thin films, effect of annealing temperature, comparison of Ag and Al electrodes for S/D electrodes were investigated.

Chapter 3 focuses on the characterization of solution-processed high-*k* dielectrics and the effect of high capacitance dielectrics on the oxide and organic TFT characteristics. Al_2O_3 and ZrO_2 layers were used for high-*k* dielectrics and the interface properties with oxide and organic semiconductors were studied. Analysis of dielectric dispersion behavior of dielectric film and all solution-processed low-voltage IGZO TFTs are covered in this chapter.

Chapter 4 covers the organic/inorganic hybrid approach to CMOS-type inverter

implementation and the investigation of potential to circuit applications. High-*k* dielectric was introduced to improve the electrical characteristics of the CMOS-type inverter.

Chapter 5 summarizes the investigation of the effect of high-*k* dielectrics fabricated by solution-process on the low-voltage TFTs and the organic/inorganic hybrid CMOS-type inverters.

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Chapter 2 High-Performance Inkjet-Printed IGZO TFTs

2.1 Introduction

Zinc-oxide (ZnO)-based materials have been widely investigated as an active layer of thin film transistors (TFTs) and a transparent conductive oxide (TCO) due to their high mobility and optically high transparency related with the wide band gap and application to solution-process [1-11]. Also, owing to an amorphous structure property, ZnO-based materials have a merit of high uniformity. Many kinds of ZnO-based materials such as ZnO [1-2], gallium-zinc-oxide (GZO) [3-4], zinc-indium-oxide (ZIO) [5-6], zinc-indium-tin-oxide (ZITO) [7], zinc-tin-oxide (ZTO) [8-9] and indium-gallium-zinc-oxide (IGZO) [10-11] have been reported for the use of active layers and TCOs. However, even though their solubility, most devices have been fabricated by expensive vacuum processes such as pulsed laser deposition (PLD) and sputtering method [1, 5-6, 9-11].

Recently, solution-based processes have been extensively studied for electronic devices because of low manufacturing cost by reducing the process steps and low

process temperature. Inkjet printing method is one of the solution-based processes, which has advantages of maskless patterning due to direct pattern definition, non-vacuum process, large area manufacturing, high throughput and economical use of the inks. In the fabrication of inkjet-printed TFTs, silver inks have been widely used for electrodes because of relatively low cost compared to gold ink and good conductivity compared to polymer conductors [12]. As an active layer, many groups have attempted to demonstrate solution-processed TFTs using an amorphous IGZO semiconductor [13-17]. However, most IGZO films were deposited by spin-coating, so that additional processes were added to pattern the active area. Several papers have been reported that inkjet-printed IGZO film, but almost electrical device performances, which are shows the mobility below 0.06 $cm^2/V•s$, are not comparable to spin-coated IGZO TFTs [15-16]. Additionally, all of the reported the inkjet-printed IGZO TFTs, inkjet-printing technology was only used for the deposition of semiconductor layer and source/drain (S/D) electrodes were deposited by a sputtering instead of inkjet-printing methods [15-17]. In the point of view of all inkjet-printed oxide TFTs and electronic circuits, the implement of both inkjet-printed IGZO active layer and silver electrodes with high electrical performance is an essential process step.

In this chapter, I report inkjet-printed IGZO TFTs, where both active layer and S/D electrodes were inkjet-printed. Heavily boron doped p-type Si substrate and thermally-grown SiO_2 were used for gate and gate insulator, respectively. IGZO semiconductor was inkjet-printed on the gate insulator using a precursor type solution and thermally annealed with various temperatures. And silver electrodes

were inkjet-printed on the active layer. To improve a performance of TFTs, carefully optimized both jetting and wetting conditions were required. Also, to investigate a crystallinity of inkjet-printed IGZO film, X-ray diffraction (XRD, D8-Advance) analysis and field emission scanning electron microscope (FESEM, S-48000) were performed. In addition, X-ray photoelectron spectroscopy (XPS, AXIS-HS) and thermogravimetric analysis (TGA, TGA Q500) were performed to investigate the annealing temperature effect.

2.2 Experiments

2.2.1 Device Structure and Process Flow

Bottom gate and top contact structure of IGZO TFTs were fabricated with both IGZO active layer and silver (Ag) S/D electrodes that were deposited and direct-patterned by inkjet-printing on SiO_2 gate dielectric. The channel width (W) and length (L) were 2,000 μm and 65 μm, respectively. Before the deposition of IGZO semiconductor layers, heavily doped p-type Si substrate was cleaned in ultra-sonicator bath. After the cleaning, IGZO layer was inkjet-printed on SiO_2 gate dielectric and thermally annealed in a furnace. Finally, Ag S/D electrodes were inkjet-printed on IGZO layer and cured in convection oven. For comparison, we also fabricated the spin-coated IGZO layer with inkjet-printed Ag S/D electrodes as well as the Figure 2.1 illustrates the sequence of fabrication process of inkjet-printed IGZO TFT.

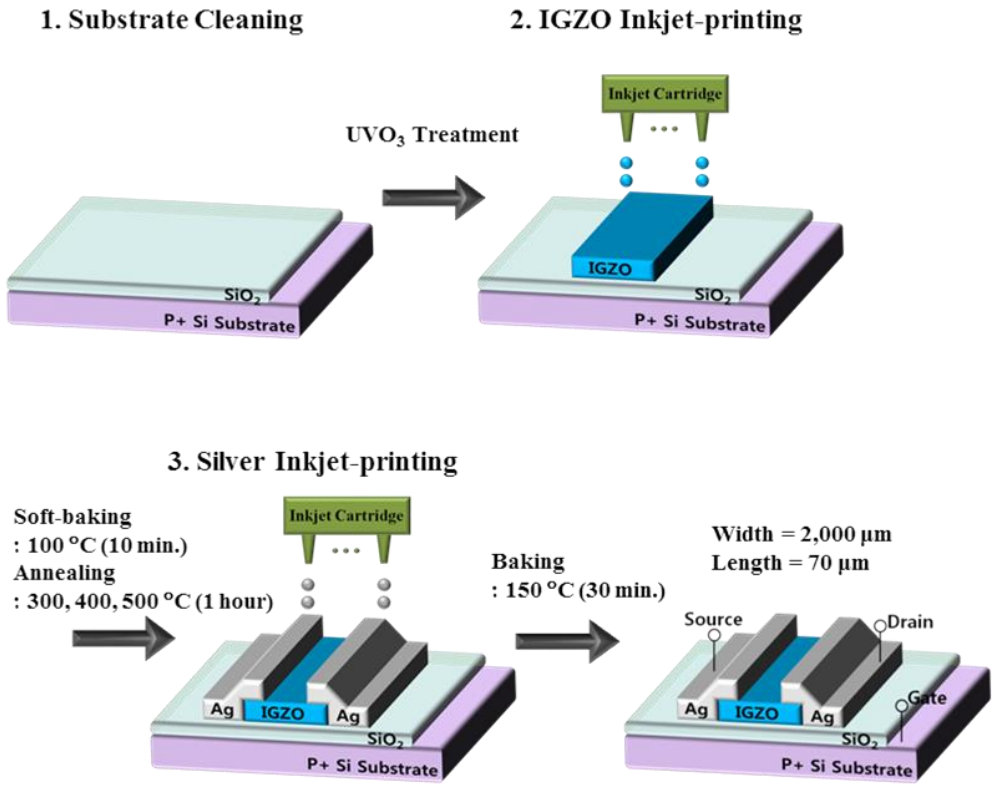


Figure 2.1 Illustration of fabrication processes of inkjet-printed IGZO TFT on the heavily doped p-type Si substrate with thermally grown SiO_2, where both IGZO layer and silver electrodes were inkjet-printed and schematic image of bottom gate and top contact structure.

2.2.2 Substrate Cleaning and Surface Treatment

Heavily boron doped p-type Si substrate and thermally-grown SiO_2 with thickness of 200 nm were used for the gate electrode and gate insulator, respectively. Heavily doped p-type Si substrate was cleaned sequentially with acetone, isoprophyl alcohol (IPA) and deionized (DI) water in the ultra-sonicator at 40 ^{o}C for 20 min, respectively. To improve the wetting property of IGZO ink on the SiO_2 surface, a surface treatment was performed. In other words, the optimization of surface energy of SiO_2 surface was needed because of hydrophilic property of IGZO solution. Before inkjet printing of IGZO films, ultraviolet (UV) ozone treatment was performed on the surface of SiO_2 for 5 min to lower the surface energy with cleaning the remained organic particles, so that the surface of SiO_2 surface was modified more hydrophilic.

2.2.3 Inkjet-Printing of IGZO Active Layer

A precursor type IGZO solution was prepared (Sigma-Aldrich) by indium acetate [$In(C_2H_3O_2)_3$], gallium nitrate hydrate [$Ga(NO_3)_3 \cdot xH_2O$] and zinc acetate dihydrate [$Zn(CH_3COO)_2 \cdot 2H_2O$] powders as precursors and 2-methoxyethanol (2ME) as a solvent. As a stabilizing agent, ethanolamine was used. . The molar ratio of indium:gallium: zinc was 3: 1: 2 and the concentration of the solution was 0.2 M. The solution was stirred at 55 ^oC for 1 hour, then, aged for 24 hours before injecting into a cartridge unit through 0.45 μm hydrophilic filter. In Figure 2.2, the preperation and image of IGZO solution is summarized. We used the piezoelectric and drop on demand type inkjet printing system (DMP-2831, Dimatix corp.) with a 10 pL cartridge (DMC-11601). 10 pL cartridge has 16 numbers of multi-nozzles and a diameter of each nozzle is about 21 μm. For the wetting property of IGZO inks, the substrate was kept at room temperature during the inkjet printing of IGZO semiconductor. Multi nozzles were used and the drop-spacing of each nozzle was adjusted 25 μm for the appropriate overlaps of each droplets. Also, a velocity of IGZO ink droplets from nozzle to surface of the substrate was adjusted about 4 m/s. Figure. 2.3 (a) shows the jetting image of inks from 5 nozzles of IGZO cartridge and the ink droplets were spherical shape due to the well controlled jetting configuration. After the printing of IGZO films, soft-baking was performed on the hot plate at 100 ^oC for 10 min to dry the solvent of IGZO. It is noted that this soft-basking process reduced the pin holes in the film. Then, the inkjet-printed samples were annealed at 300, 400, 500 ^oC for 1 hour in a furnace under atmospheric condition, respectively. With these optimized controlled jetting and wetting conditions including surface

treatment, uniform area was formed at the center of IGZO film on the SiO_2 layer, as shown in Figure. 2.3 (b), and the thickness of IGZO films were under 10 nm.

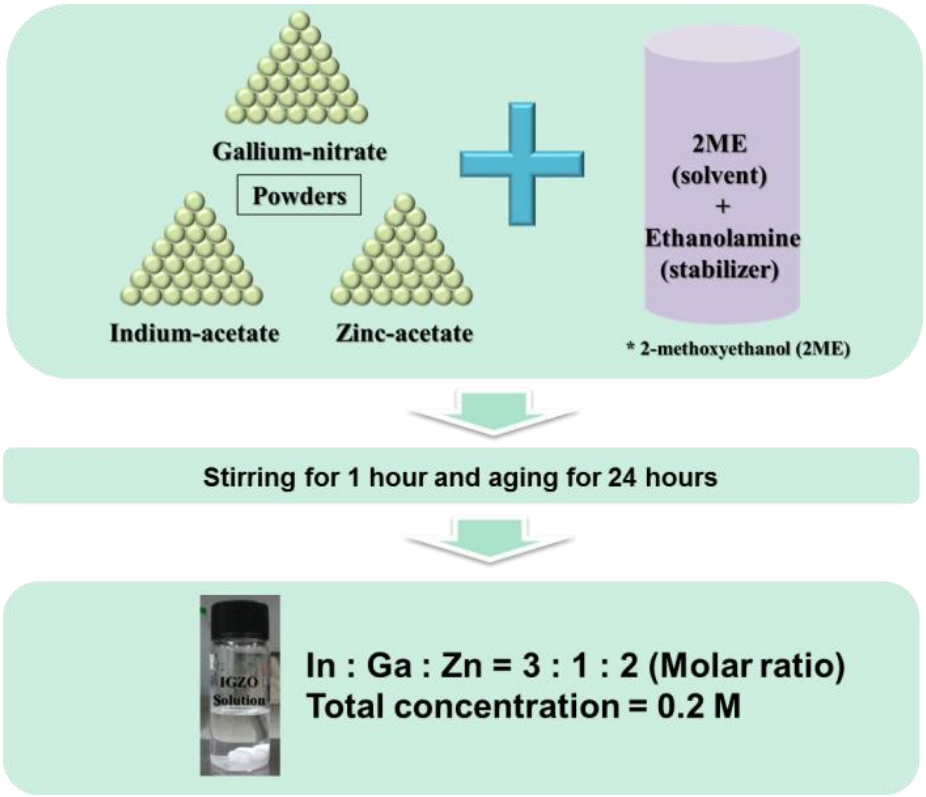
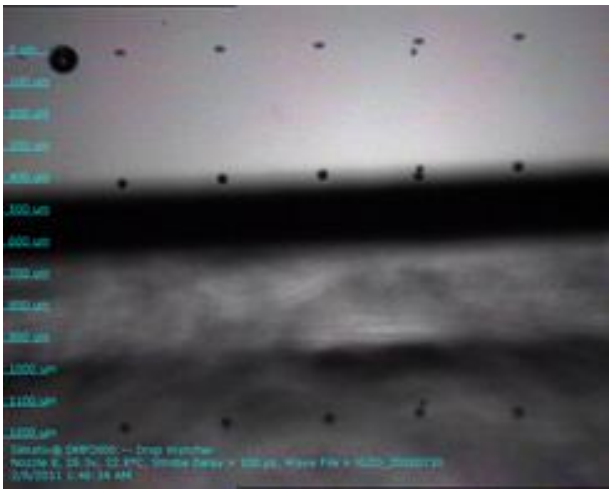


Figure 2.2 Illustration of the preparation of precursor type 0.2 M IGZO solution.



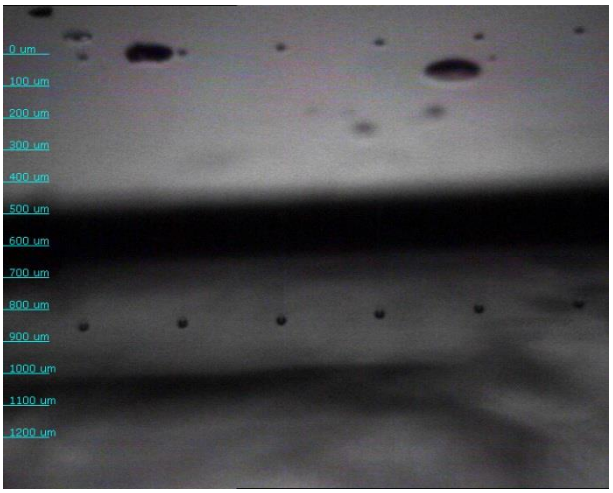
(a)

(b)

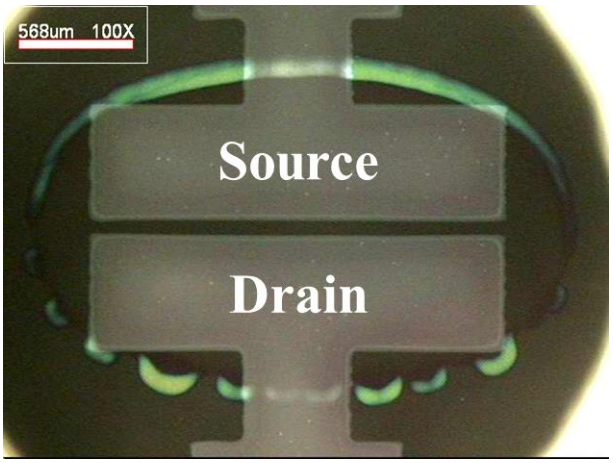
Figure 2.3 (a) Jetting image of IGZO ink using 5 nozzles with drop velocity of ~ 4 m/s. (b) Optical image of IGZO film with uniform area after the thermal annealing at 500 °C for 1 hour.

2.2.4 Inkjet-Printing of Conductive Silver Ink

To pattern the S/D electrodes on the active layer, precursor type silver ink (TEC-IJ-010, InkTec corp.) was used. During silver printing process, the substrate was kept at 60 ^{o}C. And the drop-spacing of each nozzle was adjusted to 25 μm. Figure 2.4 (a) shows the jetting image of silver inks from 6 nozzles, the ink droplets were spherical shape with the drop velocity of 8.5 m/s. To avoid unclearly defined IGZO area, the channel was intentionally formed in the uniform region as shown in Figure 2.4 (b). After the deposition of S/D electrodes, to dry the solvent of silver ink, substrates were annealed in a convection oven at 150 ^{o}C for 30 min. With the well-controlled silver inkjet-printing conditions, highly conductive electrodes were deposited on the IGZO film and the effect of edge waviness was minimized [18]. Thickness and sheet resistance of inkjet-printed silver electrodes were about 300 nm and 0.2 Ω/□, respectively [12].



(a)



(b)

Figure 2.4 (a) Jetting image of silver ink using 6 nozzles with drop velocity of ~ 8.5 m/s. (b) Optical image of silver S/D electrodes on the IGZO layer. Channel was intentionally formed the center of uniform IGZO area with width of 2,000 μm and length of 65 μm

2.3 Results and Discussion

2.3.1 Characterization of IGZO Solution and Films

For determination of thermal annealing temperature, TGA was performed from RT to 800 ^{o}C with a heating rate of 10 ^{o}C/minute. As shown in Figure 2, the weight of the precursor was decreased as the temperature increased and completed near the 400 ℃. It indicated that the metal-oxide IGZO film from the precursor solution was formed due to the thermal decomposition.

In order to investigate a crystallinity of inkjet-printed IGZO film, FESEM and XRD analysis were performed with different temperature of thermal annealed samples. FESEM results show that the crystalline orientation did not exist in IGZO films until 500 ^{o}C annealing temperature as shown Figure 2.5 (a)-(c). Also, in XRD results as shown Figure 2.5 (d), there was no significant change of peaks in the IGZO samples compare to reference sample, which is thermally grown SiO_2 film on the heavily doped p-type Si substrate. The peak located at 33 ^{o} was originated from the main peak of single crystalline Si substrate. Thus, FESEM and XRD results indicate that the inkjet-printed IGZO film was maintained amorphous structure until 500 ^{o}C. This result is well corresponded with previous research, which was reported that the solution-based IGZO film was amorphous phase until annealing temperature of 500 ^{o}C [19-20]. There are some differences of the maximum phase change annealing temperatures of amorphous IGZO films, which induced by variation of the metal composition ratios [19, 21].

Figure 2.6 shows the XPS results of inkjet-printed IGZO layer with different annealing temperatures. Dots indicate the measured data and can be divided to three main peaks. Peak 1, which located at 529.9 eV, means the oxygen in oxide lattices without oxygen vacancies and peak 2, which located at 531.4 eV, means the oxygen in oxide lattices with oxygen vacancies. Also, peak 3, which located at 531.7 eV, means the oxygen in hydroxide. Oxygen is lost from the oxide sublattice (O_o^x) to create a doubly charged oxygen vacancy ($Vo^{\bullet\bullet}$) and two free electrons. As temperature increased, the peak at 531.4 eV (red) increased but the peak at 531.7 eV (green) reduced. It indicates that IGZO films annealed at higher temperature attain more charge carriers due to thermally enhanced oxygen-vacancy formation processes.

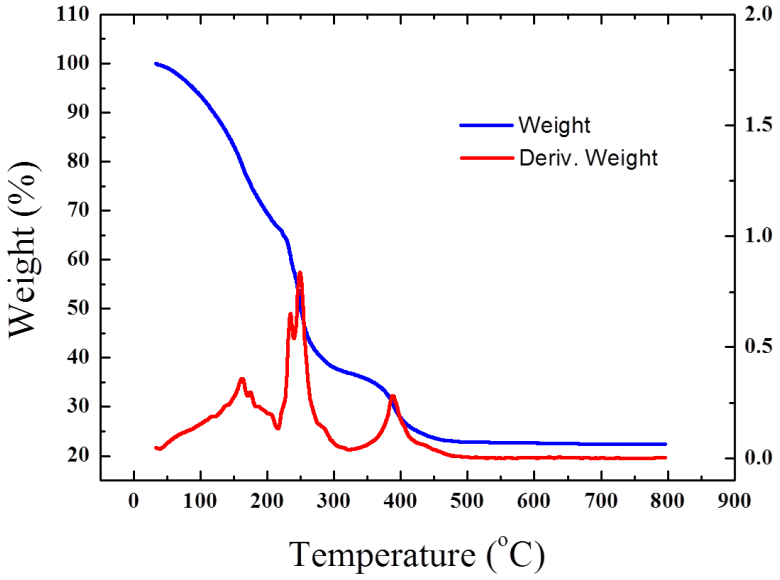
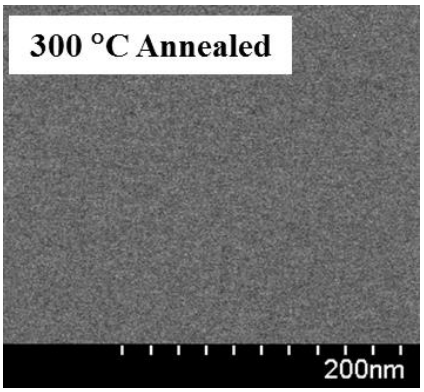
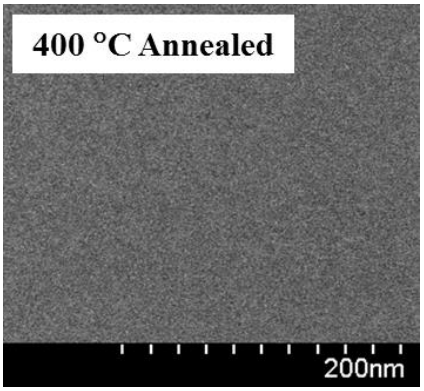


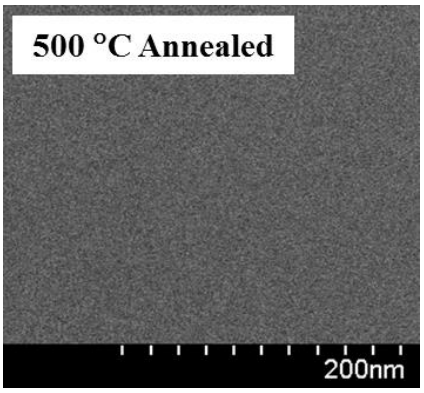
Figure 2.5 TGA result of precursor type IGZO solution with a heating rate of 10 °C/minute.


300 °C Annealed
200nm

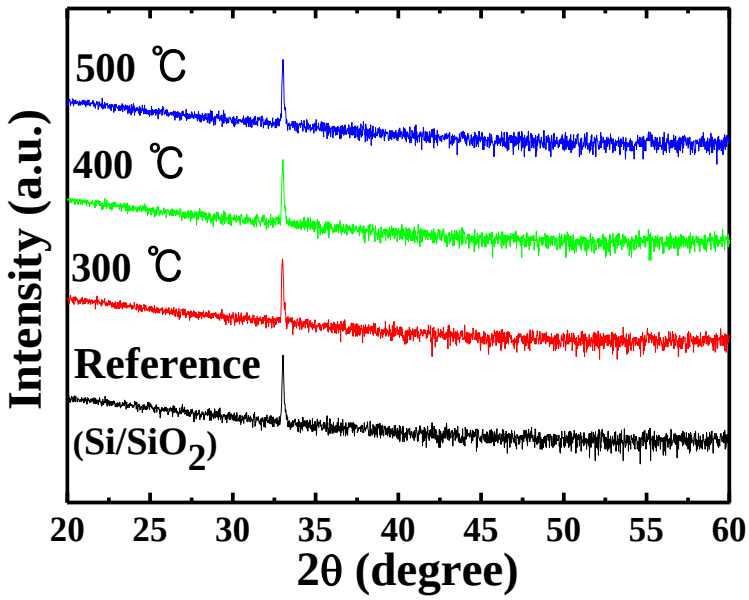
(a)


400 °C Annealed
200nm

(b)


500 °C Annealed
200nm

(c)



(d)

Figure 2.6 FESEM images of inkjet-printed IGZO film with various thermal annealing temperatures at (a) 300, (b) 400, (c) 500 ^{o}C. (d) XRD result of inkjet-printed IGZO film with various thermal annealing temperatures of 300 – 500 ^{o}C. These results indicated that the films were maintained amorphous phase until 500 ^{o}C.

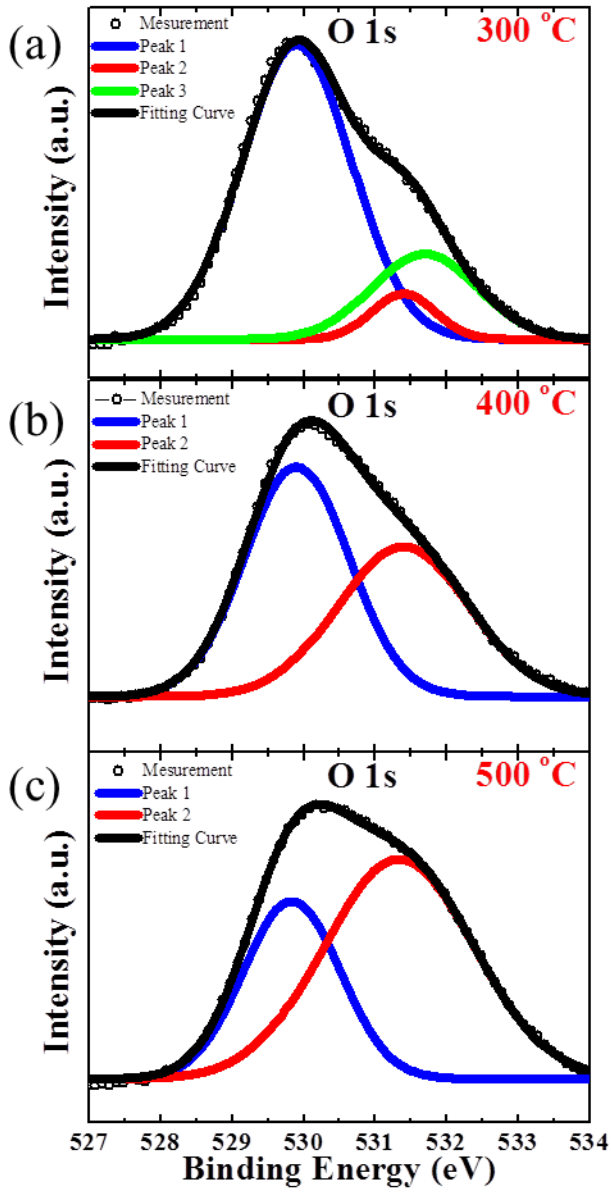


Figure 2.7 XPS results of inkjet-printed IGZO film with various thermal annealing temperatures at (a) 300, (b) 400, (c) 500 ^{o}C.

2.3.2 Effect of Annealing Temperature on Electrical Characteristics of IGZO TFTs

Figure 2.8-10 show device performances of the inkjet-printed IGZO TFTs with various annealing temperatures. The saturation mobility (μ_{sat}) and threshold voltages (V_{th}) were extracted by linear fitting of square root of drain current in the saturation region, V_{DS} = 40 V, using the following equation (1),

$$I_{DS} = \frac{1}{2}\mu_{sat} C_{ox} \frac{W}{L}(V_{GS} - V_{th})^2 \qquad (1)$$

where I_{DS} is the drain current, C_{ox} is the capacitance per unit area of SiO_2 gate insulator, V_{GS} is the gate to source voltage, W is the channel width, and L is the channel length. Also, the value of sub-threshold slope was extracted in the linear region, V_{DS} = 1 V, using the below equation (2).

$$S.S. = \frac{\partial V_{GS}}{\partial \log I_{DS}} \qquad (2)$$

We observed that all of the TFTs were operated well under gate voltage and drain voltage bias sweep. However, device performances were dependent on the thermal annealing conditions. With the annealing temperature conditions of this work, the mobility was varied from 0.574 to 3.77 cm^2/Vs and turn-on voltage (V_{ON}), which is defined the gate voltage when the drain current is over the 0.1 nA in this work, was varied in the range of 4.5 to - 5.5 V. As the increase of annealing temperature, the mobility increased up to 3.77 cm^2/Vs and V_{ON} decreased to

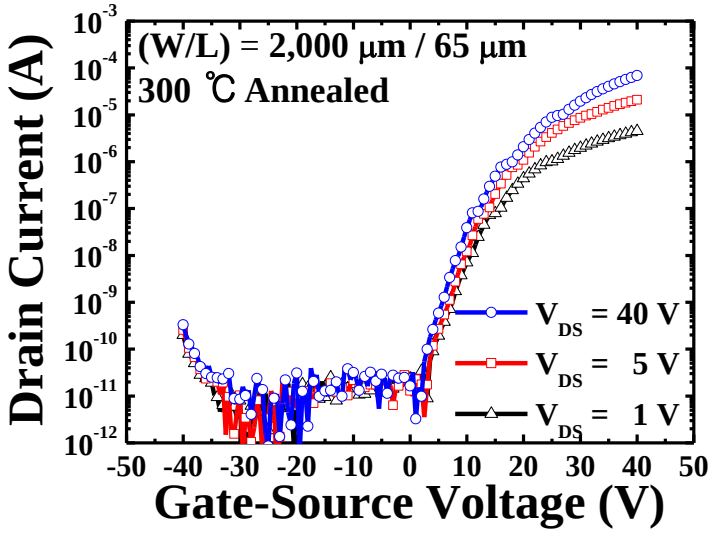
negative voltage. Figure 2.11 shows the relation of annealing temperature to the mobility and V_{ON}.

In the case of the mobility, 500 ^{o}C annealed TFT shows the highest mobility of 3.77 cm^2/Vs among the samples. On the other hand, 300 ^{o}C annealed TFT shows the lowest mobility of 0.618 cm2/V•s. Typically, the mobility is enhanced as the increase of annealing temperature due to the increase of carrier concentration by oxygen vacancies as pointed earlier [20], the rearrangement of local atoms, and the improvement of interface property between insulator and semiconductor [9, 22]. The value of mobility is comparable to the spin-coated IGZO TFTs [13-14], which showed the mobility of 1.3~5.8 cm^2/Vs, and much higher than the previously reported inkjet-printed IGZO TFTs [15-16]. High mobility was achieved due to uniform film formation by the optimized inkjet-printing conditions Relatively low mobility of 300 ^{o}C annealed IGZO TFT was attributed to the non-completion of temperature related condensation and hydrolysis reaction of IGZO solution. In TGA analysis, the temperature related reaction was completed near 400 ^{o}C [17, 20-21], hence the 400 ^{o}C annealed sample shows the better mobility. Also, the point of turn-on voltage was shifted negatively at the higher annealing temperature. Thus, 500 ^{o}C annealed TFT was operated in depletion mode, on the other hand, the other TFTs were operated in enhancement mode. It can be explained that the increase of carrier concentration as the temperature increased resulted in the negative shift of V_{ON}.

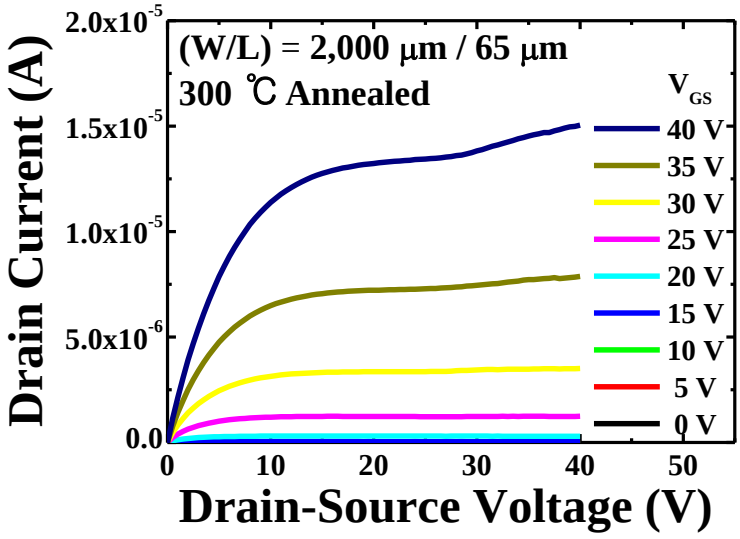
400 ^{o}C annealed TFT shows the improved sub-threshold slope, 0.490 V/dec compared with the 300 ^{o}C annealed sample, 3.22 V/dec. High S.S. value of 300 ^{o}C annealed IGZO TFT is resulted from the non-completion of reaction and the poor

interface property as mentioned above. Also, we observed that the level of off-current did not changed, less than 10^{-10} A, with the various annealing temperature. By the high mobility and the low off-current, fabricated TFTs show a good Ion/Ioff ratio up to greater than 10^{7}. It is noted that the patterned active layer prevents the leakage components from the gate leakage and the fringing effect. Electrical parameters of the fabricated TFTs are listed as Table I.

In the point of view of practical applications with a high performance inkjet-printed IGZO TFTs, the annealing temperature of 400 ^{o}C is suitable because of high mobility, enhancement mode operation, good sub-threshold slope, and high on/off current ratio. Further studies on improvement of the inkjet-printed Oxide-based TFTs are required such as contact resistance considering the work function matching between semiconductor and electrode, lowering of annealing temperature for flexible electronics.

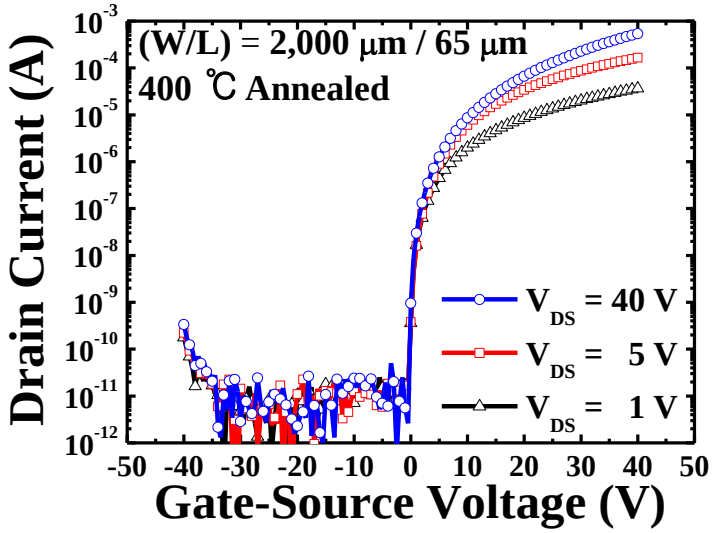


(a)

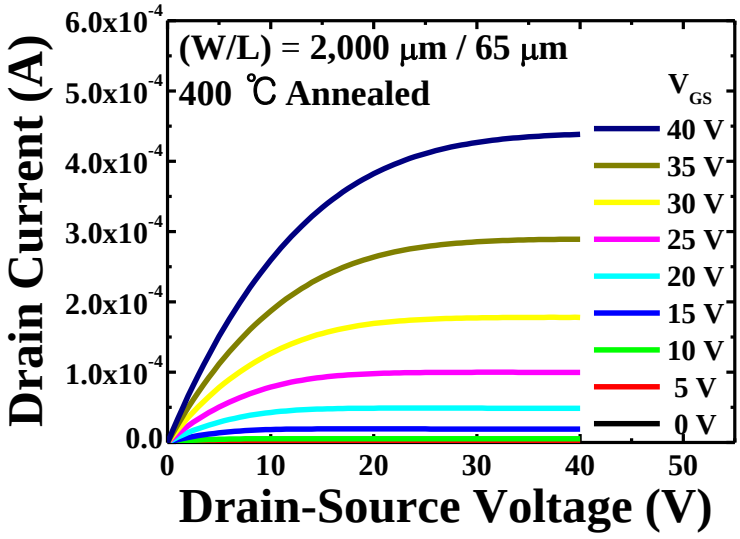


(b)

Figure 2.8 (a) Transfer characteristics and (b) output characteristics of inkjet-printed IGZO TFTs with 300 ^{o}C annealing temperatures.

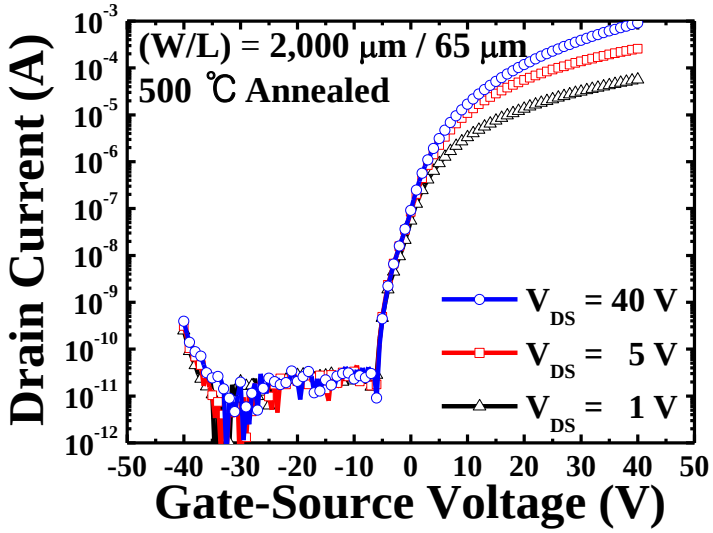


(a)

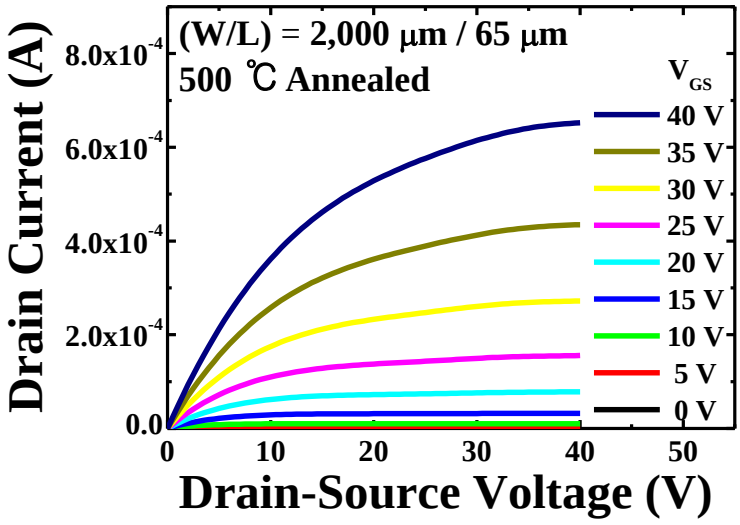


(b)

Figure 2.9 (a) Transfer characteristics and (b) output characteristics of inkjet-printed IGZO TFTs with 400 ^{o}C annealing temperatures.



(a)



(b)

Figure 2.10 (a) Transfer characteristics and (b) output characteristics of inkjet-printed IGZO TFTs with 500 ^{o}C annealing temperatures.

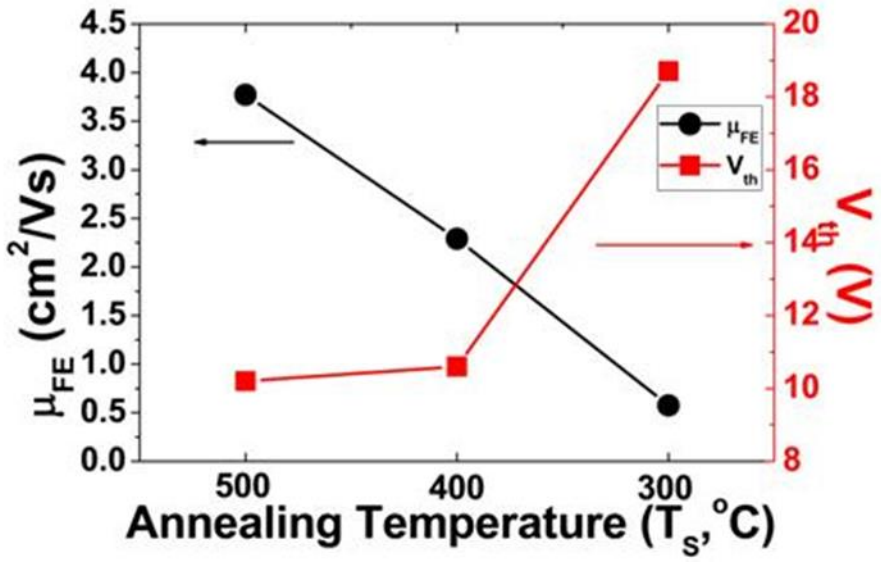


Figure 2.11 The relation of annealing temperature to the mobility (left) and turn-on voltage (right).

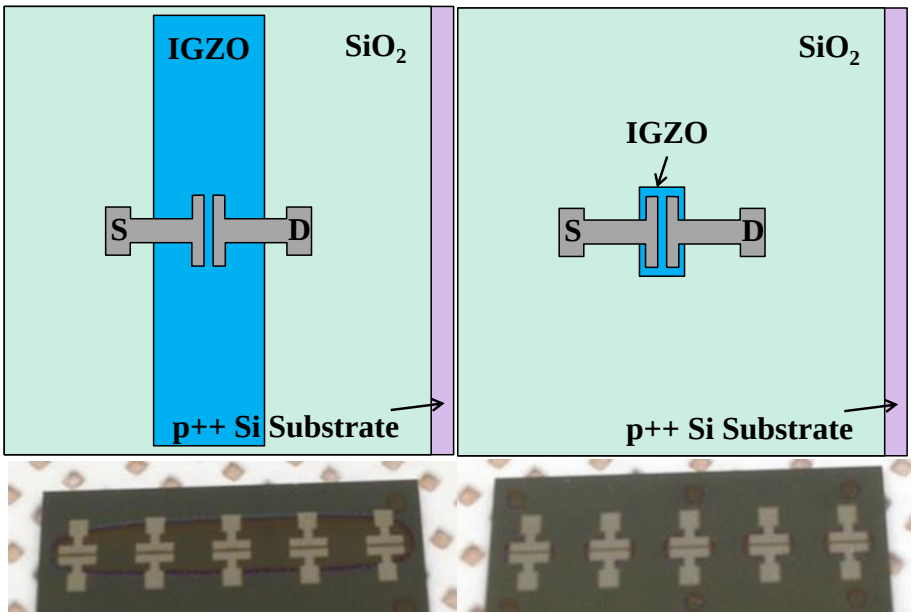
Table 2.1 Summary of electrical parameters of inkjet-printed IGZO TFTs

Annealing Temperature [°C]	**Mobility [$cm^2/V{\cdot}s$]**	**V_{ON} [V]**	**Vth [V]**	**S.S. [V/dec]**	**I_{on}/I_{off}**	**Gate leakage [A]**
300	**0.574**	**4.5**	**18.7**	**3.22**	**$> 10^6$**	**$\sim 10^{-10}$**
400	**2.29**	**0**	**10.6**	**0.490**	**$> 10^7$**	**$\sim 10^{-10}$**
500	**3.77**	**-5.5**	**10.2**	**1.10**	**$> 10^7$**	**$\sim 10^{-10}$**

2.3.3 Effect of IGZO Pattern Size on TFT Characteristics

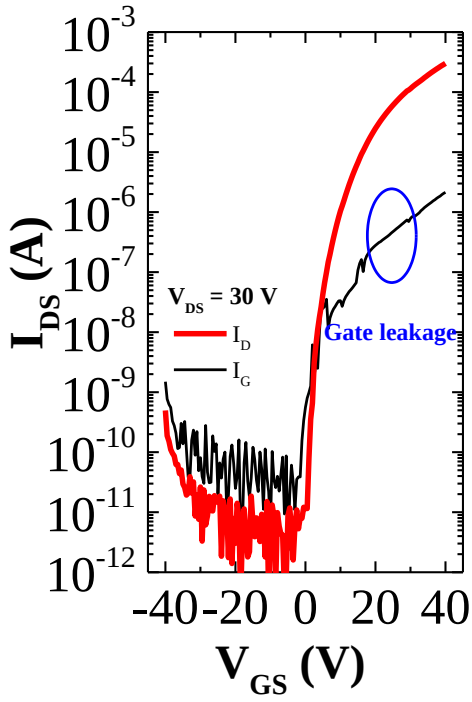
We fabricated two types of inkjet-printed IGZO TFTs with different IGZO pattern size to optimize the device structure for high-performance TFTs. Figure 2.12 (a) and (b) show the structure and optical images of different pattern size IGZO active layer. In the case of large patterned IGZO TFTs, high gate leakage current measured in transfer characteristics as shown in Figure 2.13 (a). In addition, output characteristic in Figure 2.13 (b) shows the distortion of the drain current at low V_{DS} bias condition. It indicates that IGZO TFTs with large patterned active layer cannot operate at low V_{DS} due to the high gate leakage current. On the other hand, IGZO TFTs with optimized active pattern size exhibited enhanced electrical performance of reduced gate leakage current with the high drain current as shown in Figure 2.14 (a). By optimizing the active pattern size, the distortion of the drain current was disappeared in output characteristics as shown in Figure 2.14 (b).

The high gate leakage current in large patterned IGZO TFTs was resulted from the expansion of the S/D electrodes through the IGZO layer when the IGZO semiconductor active layer was accumulated at positive gate bias condition. The expanded electrodes provide the leakage paths between gate electrode and S/D electrodes through the gate dielectric [23-24]. Thus, optimization of IGZO semiconductor pattern size is required to achieve high performance IGZO TFTs with minimized the gate leakage current.

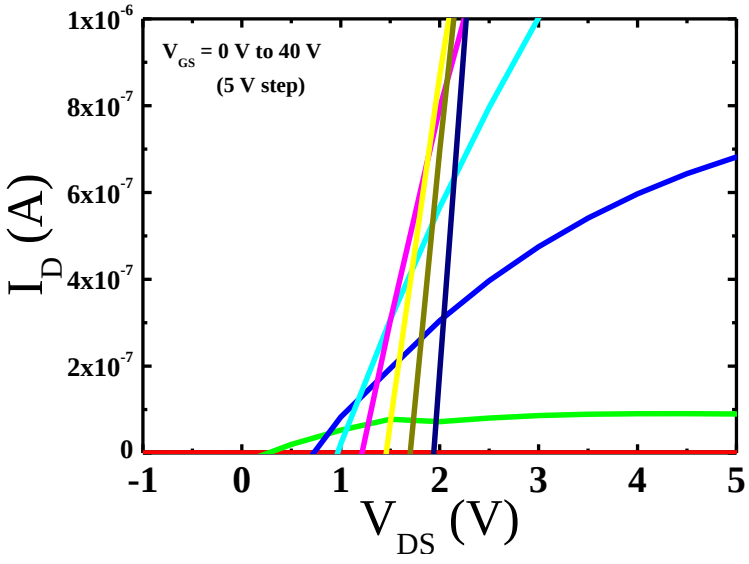


(a) (b)

Figure 2.12 Structure (top) and optical images (bottom) of (a) large patterned IGZO layer (b) optimized pattern IGZO layer.

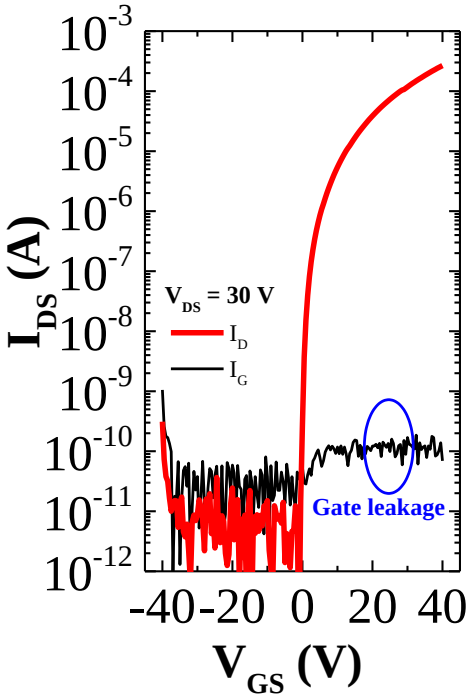


(a)

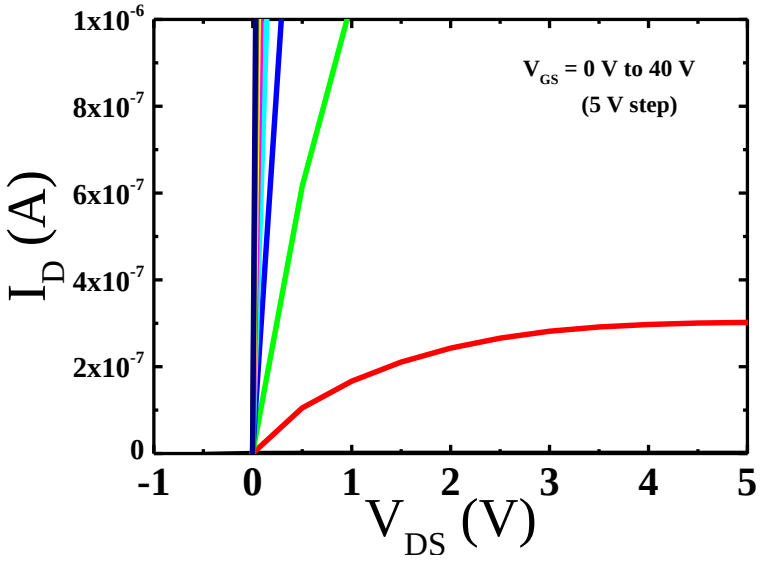


(b)

Figure 2.13 (a) Transfer characteristic with high gate leakage current and (b) output characteristics at low V_{DS} region of large patterned IGZO TFT.



(a)



(b)

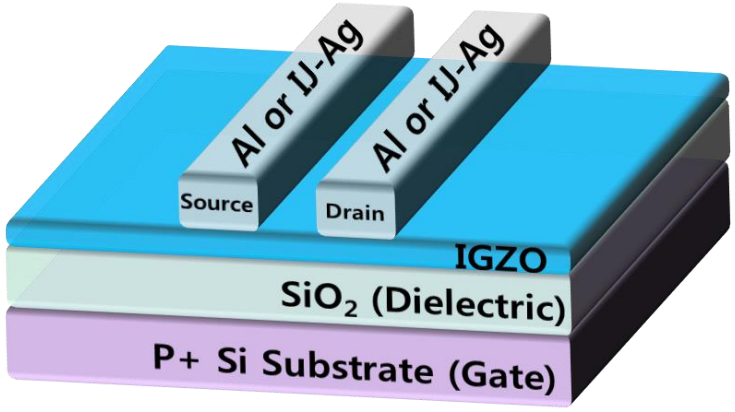
Figure 2.14 (a) Transfer characteristic with reduced gate leakage current and (b) output characteristics at low V_{DS} region of optimized active layer patterned IGZO TFT.

2.3.4 Effect of Ag S/D Electrodes on IGZO TFTs

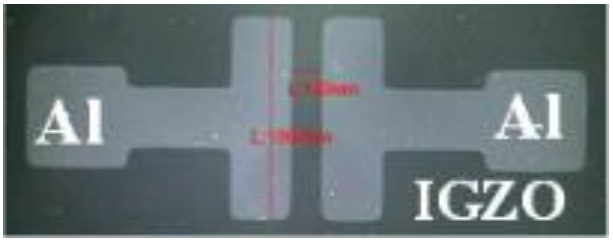
In n-type metal-oxide TFTs, Al metal has been used for S/D electrodes due to the low work function of 4.06 ~ 4.26 eV and the high conductivity. To compare inkjet-printed Ag metal and thermal evaporated Al metal for S/D electrodes, spin-coated IGZO TFTs with Al S/D electrodes were fabricated. Device structures were bottom gate and top contact. For IGZO deposition, IGZO solution was spin-coated on the UV ozone treated SiO_2 layer at 6,000 r/min for 30 s. Spin-coated substrate was soft- baked on hotplate at 100 ^oC for 10 min and then annealed at 400 ^oC for 1 hour in furnace. After the preparation IGZO film without the patterning, two types of metal were deposited on IGZO layer for S/D electrodes. One was the Al S/D electrodes (W/L = 1,000 μm/150 μm), which was deposited by thermal evaporator using shadow mask, and the other was inkjet-printed Ag S/D electrodes (W/L = 2,000 μm/100 μm). Figure 2.15 (a) and (b) show the structure of fabricated IGZO TFT and the optical image of IGZO TFT with Al S/D electrodes, respectively.

Figure 2.16 shows the transfer and the output characteristics of IGZO TFT with Al metal. The TFT shows the mobility of 1.55 cm^2/Vs, V_{th} of 12.7 V, and S.S. value of 0.363 V/dec. In the case of the inkjet-printed Ag S/D electrodes TFT as shown in Figure 2.17, the mobility, V_{th}, and S.S. value are 1.45 cm^2/Vs, 14.3 V, and 504 V/dec, respectively. From the electrical performance, TFTs with Ag S/D electrodes exhibited the compatible electrical performance to the TFT with Al S/D electrodes. Even though the large work function of Ag compared to Al electrode, the formation of Schottky contact between Ag (4.26 ~ 4.78 eV) and IGZO (4.5 eV) is difficult because of small difference in work function between Ag and IGZO [25]. We found

that contact issues at low V_{DS} region in output curves did not exist as shown in Figure 2.17 (b).

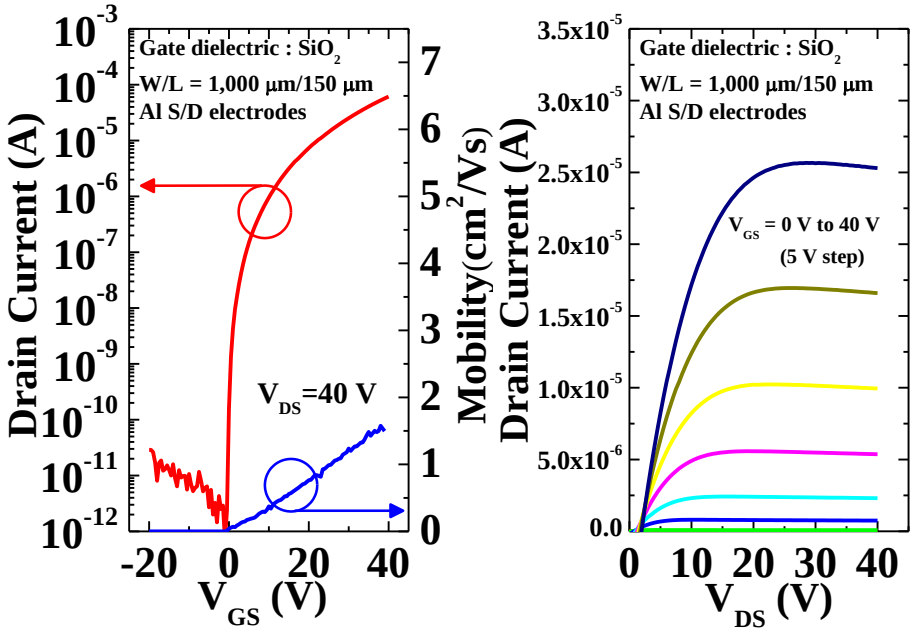


(a)



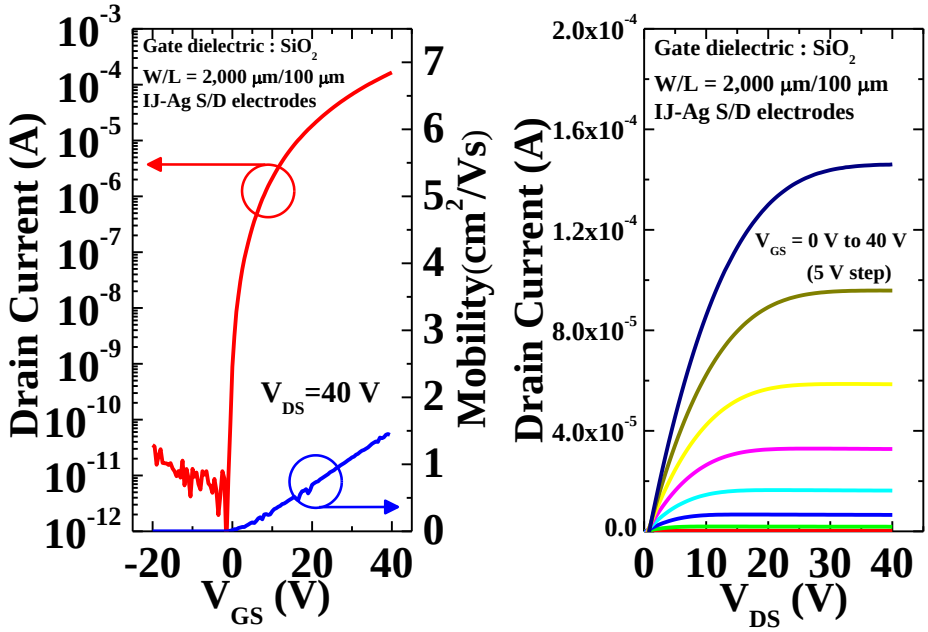
(b)

Figure 2.15 (a) Bottom gate and top contact structure of IGZO TFT with Al S/D electrodes or inkjet-printed Ag (IJ-Ag) S/D electrodes. (b) Optical image of IGZO TFT with Al S/D electrodes.



(a) (b)

Figure 2.16 (a) Transfer characteristic with mobility at V_{DS} = 40 V and (b) output characteristics of the spin-coated IGZO TFT with Al S/D electrodes.



(a) (b)

Figure 2.17 (a) Transfer characteristic with mobility at V_{DS} = 40 V and (b) output characteristics of spin-coated IGZO TFTs with inkjet-printed Ag S/D electrodes.

2.4 Summary

In conclusion, IGZO TFTs were fabricated on the heavily doped p-type Si substrate, where both active layer and S/D electrodes were inkjet-printed. Fabricated TFTs with W/L = 2,000/65 (μm/μm) shows a good field effect mobility above 2 $cm^2/V \cdot s$ and an I_{on}/I_{off} ratio greater than 10^7 at 400 °C annealing temperature. XPS result indicated that IGZO films annealed at higher temperature attain more charge carriers due to thermally enhanced oxygen-vacancy formation processes. Also, results of FESEM and XRD analysis showed that inkjet-printed IGZO films were maintained amorphous structure until 500 °C annealing temperature. For high performance IGZO TFTs, it is noted that well optimized jetting, wetting, and environmental conditions were required and active area should be minimized for reducing the leakage components. The inkjet-printed oxide TFTs can be applicable to promising future electronics including all inkjet-printed circuit and flexible display, however, it still has issues related with high process temperature. Hence, further studies on the lowering of the temperature are necessary for feasibility.

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Chapter 3 Solution-Processed High-*k* Dielectrics for High-Performance Low-Voltage TFTs

3.1 Introduction

Thin-film devices based on SiO_2 gate dielectric have been widely studied and developed over the several decades. SiO_2 gate dielectric shows excellent properties: good insulating, large energy band gap (9 eV), and low density of traps [1]. However, there still remain issues of high operating voltage related with low dielectric constant (*k*, 3.9) of SiO_2. Recently, there are many efforts for reducing the operational voltage of TFTs using high capacitance dielectrics [2-8]. By incorporating the high capacitance dielectrics, more charges can be accumulated at dielectric and semiconductor interfaces at the same bias condition, hence, TFTs and circuits can be operated under a low voltage condition. Additionally, low-power consumption and high electrical performance including a low subthreshold swing can be achieved. Various high dielectric constant (high-*k*) materials have been researched for application as a dielectric layer of TFTs. The high-*k* materials can be categorized into three types: inorganic dielectrics, organic dielectrics, and hybrid dielectrics as shown in Figure 3.1. The inorganic dielectrics refer to metal oxide

based high-*k* gate dielectric materials (Al_2O_3, ZrO_2, HfO_2, etc.). And the organic dielectrics include the polymer dielectrics and self-assembled mono- and multilayers. Also, hybrid dielectrics mean the use of both organic and inorganic materials for taking advantages of good interface property of organic material and high capacitance of inorganic material. However, organic materials are prone to degrade in thermal and chemical reaction. Thus, inorganic dielectrics are appropriate materials for high temperature processed metal oxide semiconductors. In inorganic dielectrics, several parameters such as k value, thermodynamic stability, crystalline or amorphous phase, interface quality, band offset and defects should be considered. Figure 3.2 shows the inverse relationship of k value and band gap in various materials. It is noted that high-*k* materials induce more charges at interface in same condition, however, the insulating property, which is related with band gap, get worse as the increase of k value. Among the inorganic dielectrics, zirconium oxide (ZrO_2) and aluminum oxide (Al_2O_3) are representative materials of high-*k* oxide dielectrics due to their high dielectric constant, relatively large band gap, and solution processing possibility.

As pointed out earlier, solution-based processes have advantages of low manufacturing cost, non-vacuum, and easy process. To date, however, there are only few papers reporting the low-voltage TFTs using solution-processed high-*k* oxide gate dielectric even though a lot of papers about low-voltage TFTs with the high-*k* oxide dielectric using vacuum deposition such as sputtering and atomic layer deposition have been reported. In this Chapter 3, we demonstrated the solution processed high-*k* dielectrics and their effects on oxide and organic TFT characteristics. And investigation on a metal-insulator-semiconductor-metal (MISM) capacitor and a metal-insulator-metal (MIM) capacitor revealed that the origin of the high-performance of TFTs was the formation of electric double layer (EDL) in Al_2O_3 dielectric under the IGZO layer.

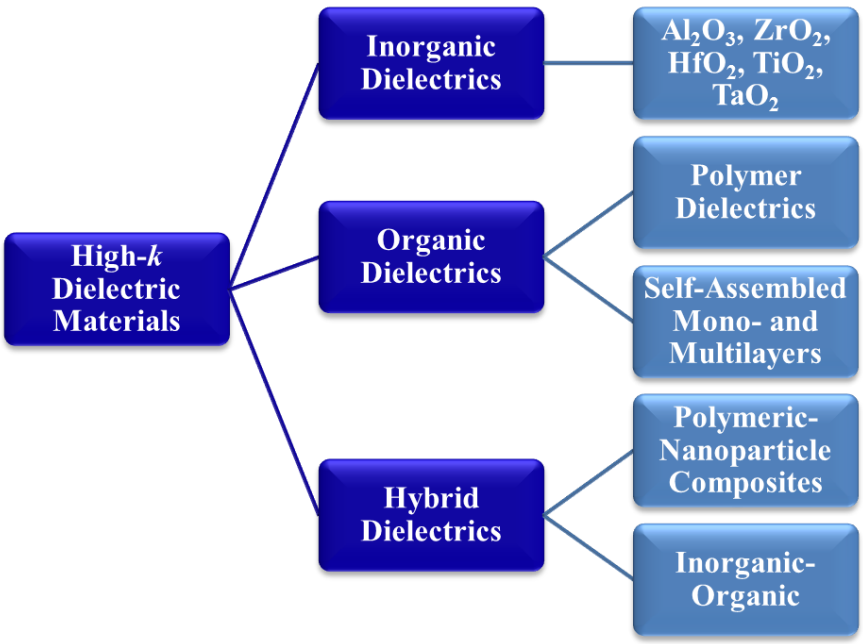


Figure 3.1 Categorization of high-k dielectric materials into 3 types: inorganic, organic, and hybrid.

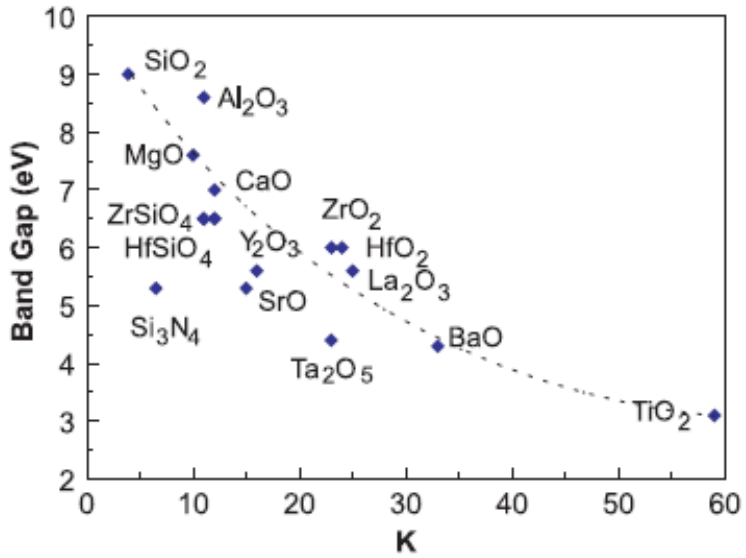


Figure 3.2 The relationship of energy band gap and dielectric constant. (ref. [1]).

3.2 Low-Voltage IGZO TFTs

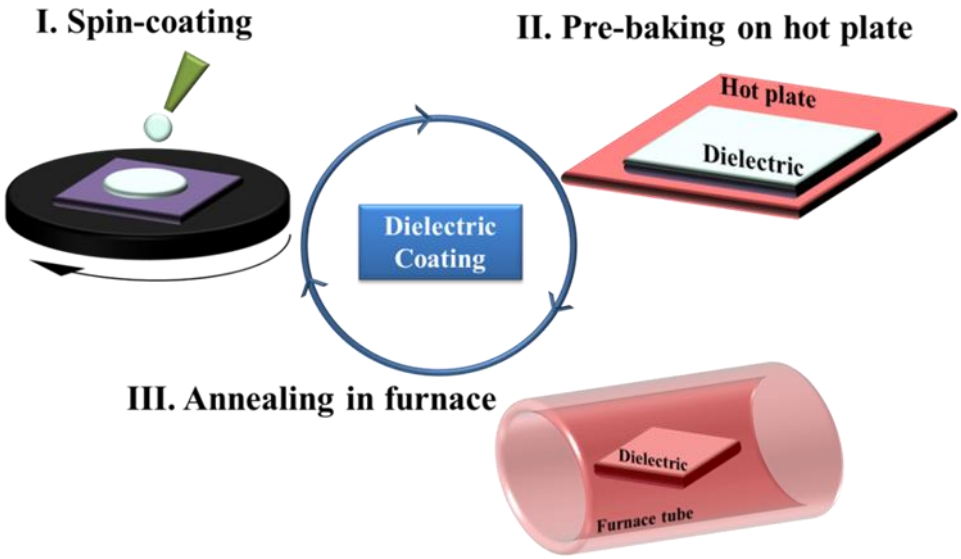
3.2.1 Fabrication of High-*k* Dielectrics and TFTs

Al_2O_3 and ZrO_2 high-*k* dielectrics were fabricated on the heavily boron-doped p-type Si substrates, which was used as gate electrode, by solution-process with precursor-type solutions. The solution of Al_2O_3 was prepared by dissolving 0.1 M aluminum nitrate nonahydrate [$Al(NO_3)_3 \cdot 9H_2O$] powder in 2-methoxyethanol [$CH_3OCH_2CH_2OH$]. And the ZrO_2 solution was prepared by dissolving 0.5M zirconium chloride [$ZrCl_4$] and zirconium isopropoxide isopropanol complex [$Zr(OCH(CH_3)_2)_4 \cdot (CH_3)_2CHOH$] with a molar ratio of one in 2-methoxyethanol [$CH_3OCH_2CH_2OH$]. The solutions were stirred at 55 ^oC for 1 hour with 600 r/min, then, aged for 24 hours.

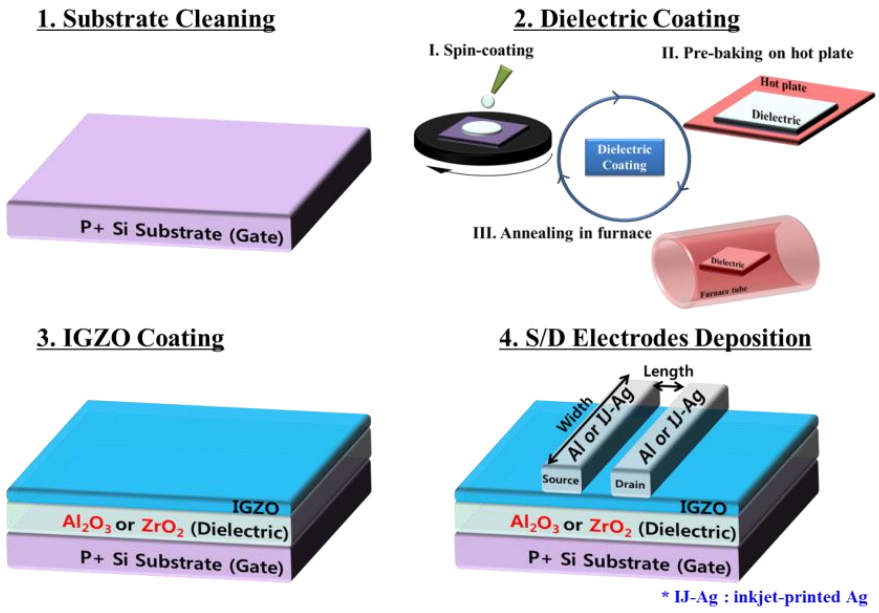
For deposition of dielectrics, simple and fast spin-coating was used. Al_2O_3 layer was spin-coated on the heavily doped p-type Si substrate with 3000 r/min for 30 seconds in ambient condition after the native oxide was removed, then, soft-baking and annealing were proceeded on hot plate for 80 ^oC for 10 min and in furnace for 500 ^oC for 4 hours, respectively. And ZrO_2 layer was spin-coated on the substrate with 2000 r/min for 30 sec and soft-baekd on the hotplate at 200 ^oC for 1 h in Ar_2-filled glove box due to prevent rapid evaporation of HCl gas. Then, ZrO_2 film was thermally annealed in the furnace 500 ^oC for 1 hours in ambient air condition. After annealing, the spin-coating and annealing processes were repeated once to achieve a desired thickness. The deposition processes of high-*k* dielectrics are illustrated in Figure 3.3 (a).

For the fabrication of MIM capacitors, Au electrodes were deposited by thermal evaporator and inkjet-printed Ag electrodes were used for the top electrodes of MIM capacitors. As shown in Figure 3.3 (b), the bottom gate and top contact structure of IGZO TFTs were fabricated onto the solution-processed high-*k* gate insulator. After the preparation of high-*k* dielectrics, the precursor type 0.2 M IGZO

n-type semiconductor solution was spin-coated on the dielectric and annealed at 400 ^{o}C in the furnace. The Al S/D electrodes (W/L = 1,000 μm/150 μm) were deposited by thermal evaporation on the IGZO layer with Al_2O_3 high-*k* dielectric and the Ag S/D electrodes (W/L = 2,000 μm/100 μm) were inkjet-printed on the IGZO layer with ZrO_2 high-*k* dielectrics.



(a)



(b)

Figure 3.3 (a) Coating processes of high-*k* dielectric with spin-coating and thermally annealing. (b) Fabrication process of low-voltage IGZO TFTs on high-*k* dielectrics.

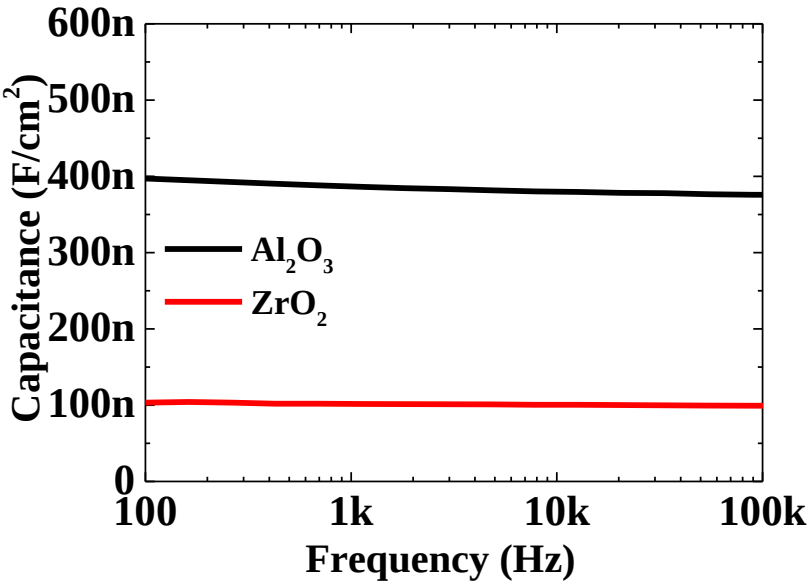
3.2.2 High-*k* Film and MIM Capacitor Characteristics

Figure 3.4 (a) and (b) shows the MIM capacitor characteristics of both Al_2O_3 with Au electrodes and ZrO_2 with IJ-Ag electrodes. In capacitance-frequency (C-*f*) characteristics, Al_2O_3 and ZrO_2 MIM capacitors show the capacitance of 379 and 100 nF/cm^2, respectively, as shown in Figure 3.4 (a). And the Al_2O_3 and ZrO_2 MIM capacitors have the leakage current density of 2×10^{-6} and 1×10^{-8} A/cm^2 bias at 5 V, respectively, as shown in Figure 3.4 (b). The differences of capacitance and leakage current density between two films are originated from the film thickness and the dielectric constant. Thicknesses of Al_2O_3 and ZrO_2 films were 15 nm and 160 nm, respectively.

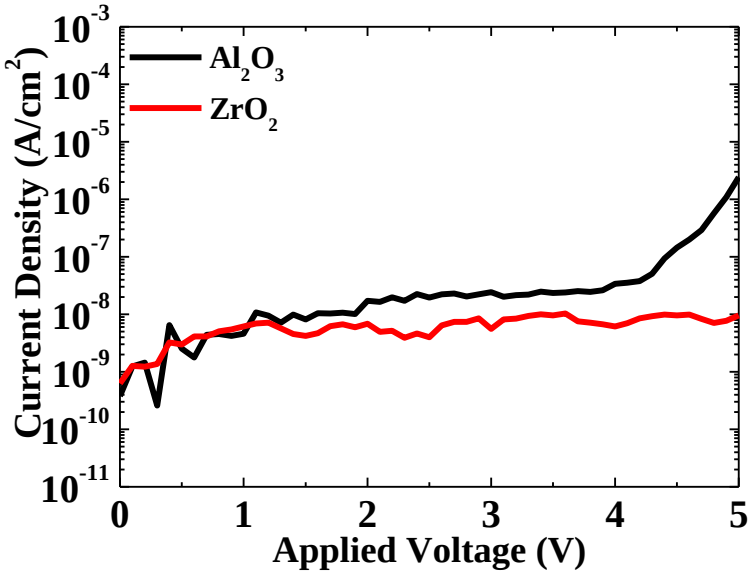
XRD was performed for the phase analysis of the dielectrics. Al_2O_3 dielectric film shows the amorphous phase even though thermal annealing was processed at high temperature as shown in Figure 3.5 (a). On the contrary, ZrO_2 dielectric film shows the polycrystalline phase, which is mixture of tetragonal and monoclinic phase as shown in Figure 3.5 (b). The AFM images and profiles of cross-sectional roughness of Al_2O_3 and ZrO_2 layers are shown in Figure 3.6 (a) and (b), respectively. Al_2O_3 film shows the very smooth surface properties, peak-to-valley of 2.43 nm and rms roughness of 0.183 nm. However, ZrO_2 film shows the poor surface properties, peak-to-valley of 9.63 nm and rms roughness of 1.25 nm.

Capacitance, leakage property, and film morphology are key factor to the choice of high-*k* dielectric film for TFTs. High capacitance can induce more charges at the semiconductor/dielectric interface at the same gate bias, thus it can enable to reducing the operating voltage of TFTs. And leakage current density, especially gate leakage current through the dielectric, should be suppressed. High leakage current can cause the high power dissipation as well as poor transistor characteristics. Also, polycrystalline morphology is undesirable because grain boundaries in polycrystalline gate dielectrics can cause the high leakage current due to the presence of leakage paths, hence the amorphous phase property is much preferred to

the use of gate dielectrics in transistors. Besides, smooth surface property is required to reduce the carrier scattering.

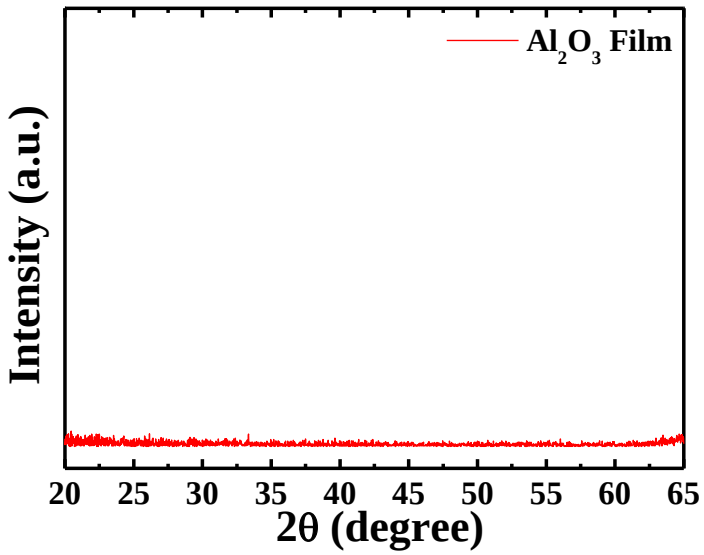


(a)

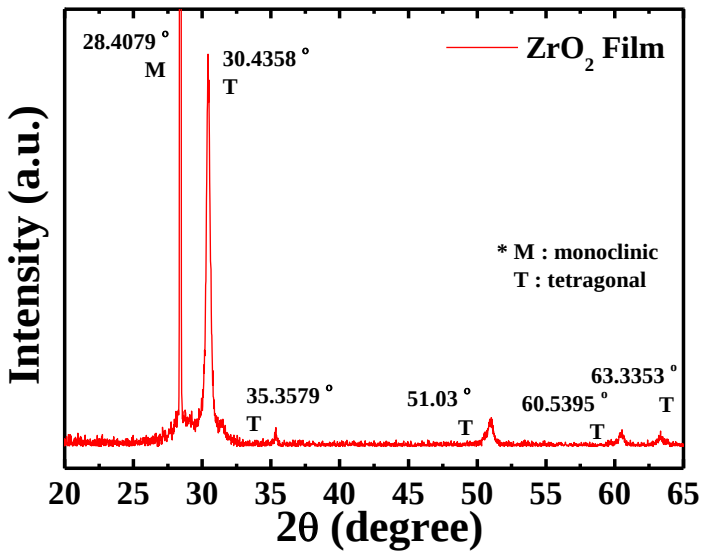


(b)

Figure 3.4 Electrical characteristics of solution-processed high-*k* Al_2O_3 and ZrO_2 MIM capacitors: (a) capacitance-frequency characteristics and (b) leakage current properties

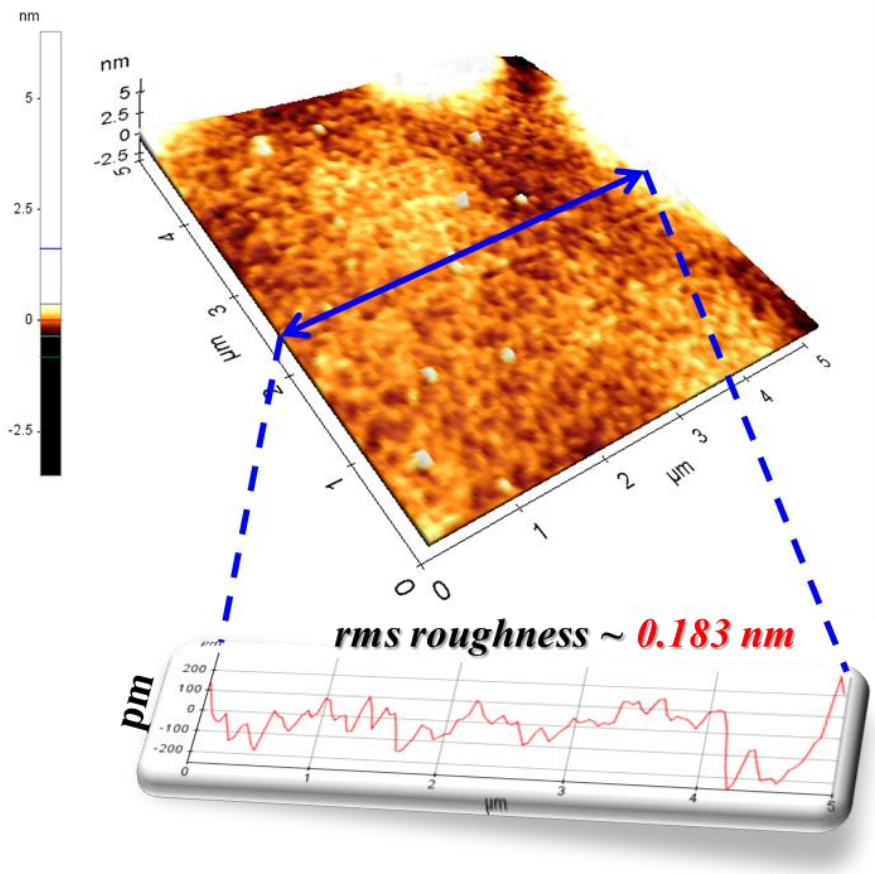


(a)



(b)

Figure 3.5 XRD results of solution-processed high-*k* dielectric: (a) amorphous phase Al_2O_3 and (b) polycrystalline phase ZrO_2


nm
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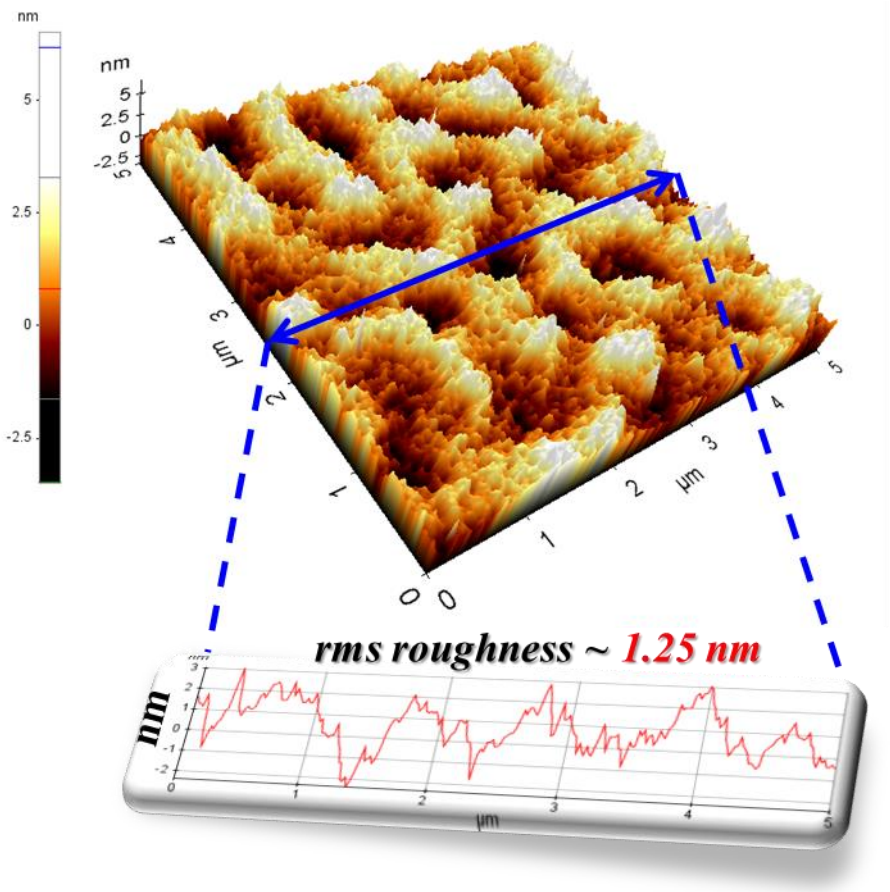
μm

(a)

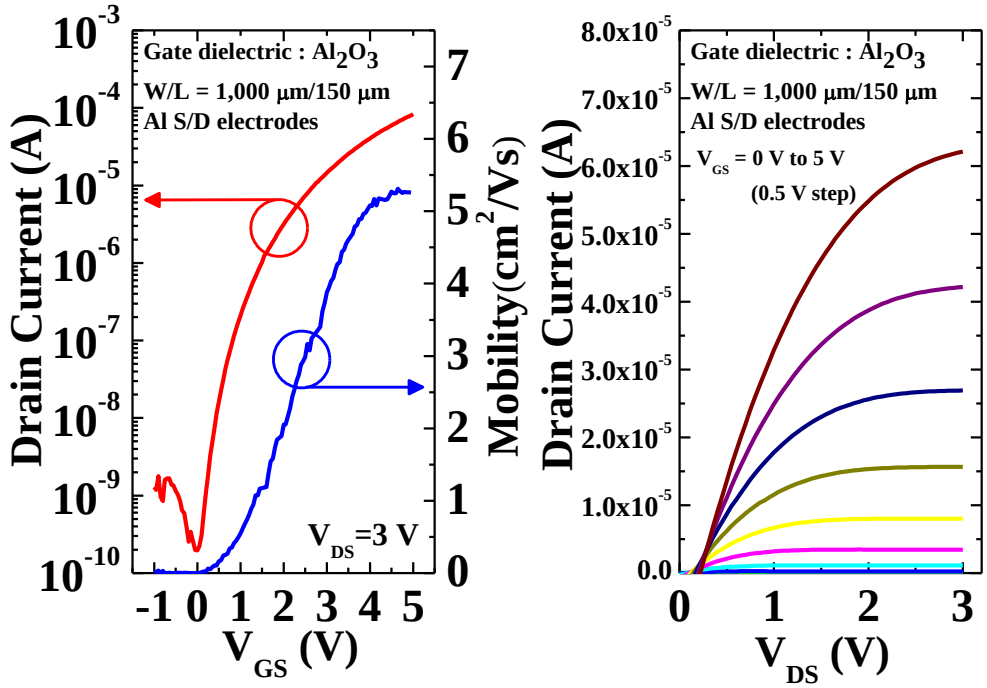


(b)

Figure 3.6 Surface morphology and roughness of solution-processed high-*k* dielectrics: (a) Al_2O_3 and (b) ZrO_2

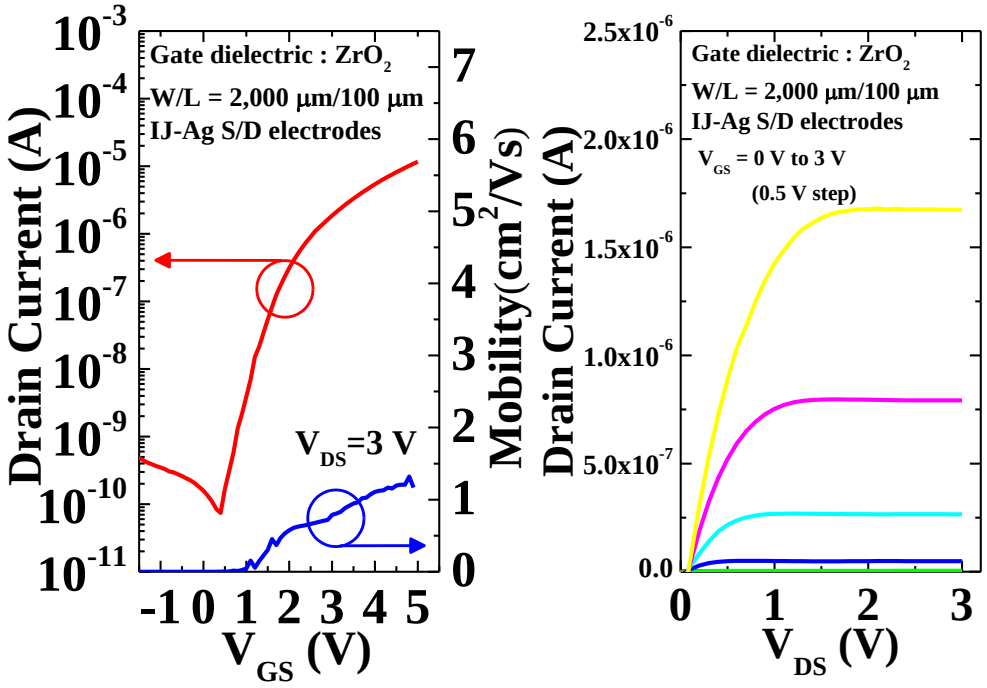
3.2.3 Low-Voltage IGZO TFTs Characteristics

Electrical behaviors of IGZO TFTs on solution-processed high-*k* Al_2O_3 dielectric are shown in Figure 3.7. TFTs on Al_2O_3 operated in low voltage range under 5 V. Low voltage operation is attributed to the high capacitance value and low leakage properties of Al_2O_3. Comparing with the IGZO TFTs on SiO_2 as shown in Figure 2.13, IGZO TFTs on Al_2O_3 exhibited high current driving capability to that of devices on SiO_2 even in low-voltage range. Furthermore, the high-*k* IGZO TFTs have the better electrical properties such as mobility of 5.28 cm^2/Vs, threshold voltage of 1.70 V, and S.S. of 196 mV/dec comparing parameters of TFTs on SiO_2. Reduced threshold voltage (12.9 V → 1.70 V) and steep S.S. (363 mV/dec → 196 mV/dev) are originated from the high capacitance of gate dielectric layer. And high mobility is resulted from the improvement of interface between IGZO and Al_2O_3 gate dielectric. Figure 3.8 shows the electrical characteristics of IGZO TFTs on ZrO_2 gate dielectric. It also operated in low voltage condition due to the high capacitance of 100 nF/cm^2, but exhibited inferior performance compared to TFTs on Al_2O_3. It shows mobility of 1.23 cm^2/Vs, threshold voltage of 1.95 V, and S.S. of 337 mV. The main reason of deteriorated mobility and S.S. is poor interface property of IGZO and ZrO_2, which originated from the rough surface property (rms value ~ 1.25 nm) of ZrO_2 gate dielectric. Both IGZO TFTs on Al_2O_3 and ZrO_2 shows the low on-off ratio of 10^5 due to the high off current. The high off current is attributed to the non-patterned IGZO layer and leakage current density compared to SiO_2 dielectric. Electrical parameters of various IGZO TFTs are summarized in Table 2.



(a) (b)

Figure 3.7 (a) Transfer characteristics with mobility and (b) output characteristics of IGZO TFT on solution-processed Al_2O_3 dielectric.



(a) (b)

Figure 3.8 (a) Transfer characteristics with mobility and (b) output characteristics of IGZO TFT on solution-processed ZrO_2 dielectric.

Table 3.1 Electrical parameters of various IGZO TFTs.

Dielectric	C [nF/cm^2]	S/D electrode	Operating Voltage [V]	Mobility [cm^2/V·s]	Vth [V]	S.S. [mV/dec]	I_{on}/I_{off}
Al_2O_3	437	Al	5	5.28	1.70	196	$> 10^5$
SiO_2	17.3	Al	40	1.55	12.9	363	$> 10^7$
SiO_2	17.3	IJ-Ag	40	1.45	14.3	504	$> 10^7$
ZrO_2	100	IJ-Ag	5	1.23	1.95	337	$> 10^5$

3.2.4 All Solution-Processed Low-Voltage IGZO TFT

Figure 3.9 shows the fabrication process of all solution-processed low-voltage IGZO TFTs with Al_2O_3 gate dielectric. For the low-voltage operation, high-*k* Al_2O_3 gate dielectric was deposited onto the heavily doped p-type Si substrate by spin-coating with 3000 r/min for 30 seconds in ambient condition using the precursor type solution prepared by dissolving 0.1 M aluminum nitrate nonahydrate [$Al(NO_3)_3 \cdot 9H_2O$] powder in 2-methoxyethanol [$CH_3OCH_2CH_2OH$]. After the spin-coating, the sample was soft-baked on the hotplate for 80 ^oC for 10 min and then annealed in the furnace for 500 ^oC for 4 hours. For the n-type semiconductor, IGZO active layer was deposited and directly patterned by inkjet-printing. Then, sample was soft-baked at 100 ^oC for 10 min and annealed 400 ^oC for 1 hour in the furnace. Finally, Ag metal-organic ink was inkjet-printed on the IGZO layer for S/D electrodes (W/L = 1,030 μm/100 μm) and sintered at 150 ^oC for 30 min in the convection oven.

IGZO TFT operated well at low-voltage condition under 5 V. And it shows good electrical properties such as mobility of 4.03 cm^2/Vs, threshold voltage of 1.98 V, and S.S. of 148 mV/dec comparing parameters of TFTs on Al_2O_3 with Al S/D electrodes. Furthermore, the on-off ratio is over 10^6, which value is later than that of spin-coated IGZO TFT on high-*k* dielectrics. Improvement of the on-off ratio is attributed to the low off current property as shown in Figure 3.10 (a), which arises from the patterning of the active layer. In the output characteristics as shown in Figure 3.10 (b), drain current increases from the 0 V due to the low gate leakage by patterning of the active layer.

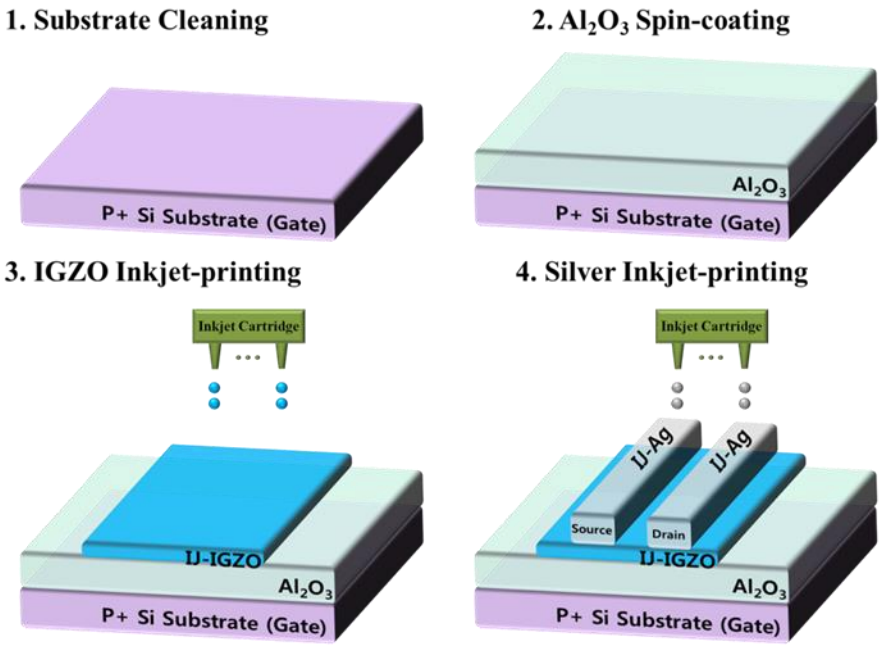
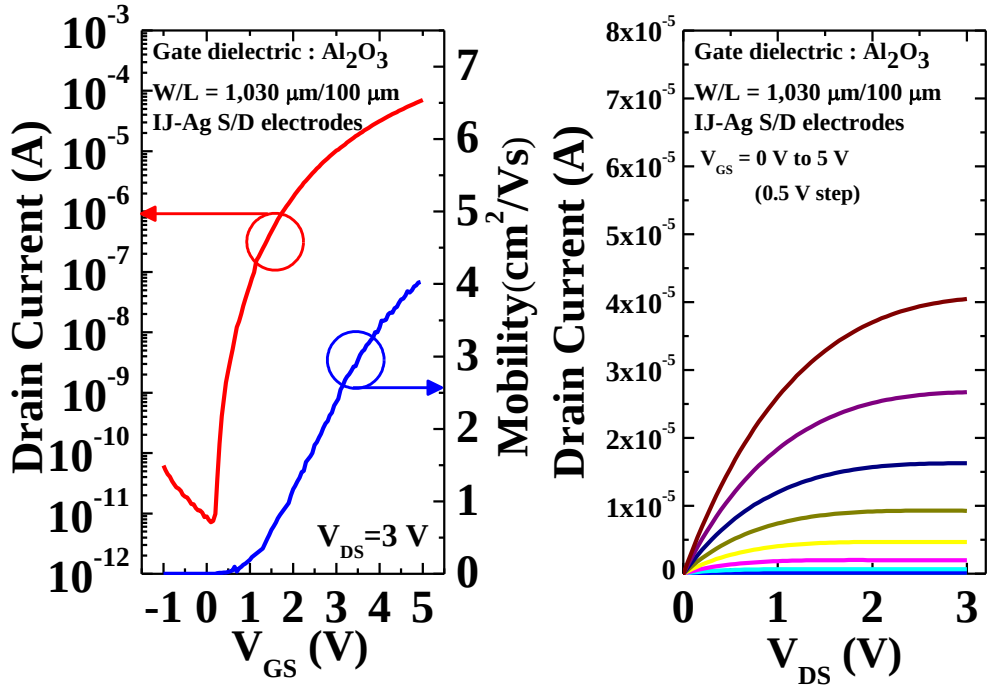


Figure 3.9 Fabrication process of all solution-processed low-voltage IGZO TFT



(a) (b)

Figure 3.10 (a) Transfer characteristics with mobility and (b) output characteristics of all solution-processed low-voltage IGZO TFT.

3.3 Dielectric Dispersion Behavior of Solution-Processed High-Performance Low-Voltage IGZO TFTs on High-*k* Al_2O_3 Dielectric

3.3.1 Experimental

IGZO TFT, Al-Al_2O_3-IGZO-p++ Si (MISM) capacitor, Al-Al_2O_3-p++ Si (MIM) capacitor were fabricated as shown in Figure 3.11. A precursor type solution was prepared (Sigma-Aldrich) dissolving an 0.5 M aluminum chloride in 2-methoxyethanol for the solution-processed high-*k* Al_2O_3 gate dielectric. Al_2O_3 film was spin-coated on the heavily doped p-type Si substrate at 3000 r/min for 30 s after the native oxide was removed. To prevent abrupt evaporation of HCl gas in Al_2O_3 precursor, coating and soft-baking at 200 ^oC for 30 min were performed in Ar_2 filled glove box. Then, film was annealed carefully 500 ^oC for 4 h in air ambient furnace. Thermally annealed Al_2O_3 film showed the thickness of 60 nm.

For the n-type metal-oxide semiconductor layer, precursor type IGZO solution was prepared (Sigma-Aldrich) by mixing indium acetate, gallium nitrate hydrate and zinc acetate dihydrate into 2-methoxyethanol with ethanolamine for stabilizing agent. The molar ratio of In: Ga: Zn was 3: 1: 2 and the concentration of the solution was 0.2 M. The solution was stirred at 55 ^oC for 1 hour, then, aged at room temperature for 24 h. IGZO solution through a hydrophilic filter was spin-coated on the ultraviolet (UV) ozone treated Al_2O_3 film at 6000 r/min for 30 s in air. It is noted that the UV ozone treatment was performed before the deposition of IGZO layer to modify the surface energy of the Al_2O_3 surface to hydrophilic. Soft-baking was performed on the hot plate at 100 ^oC for 10 min in air to evaporate the solvent of IGZO. Then, to complete the chemical reaction of IGZO, the films were annealed at 400 ^oC for 1 h in a furnace under atmospheric condition. IGZO layer was patterned by photolithography and an aluminum (Al) was deposited through the shadow masks by thermal evaporator for source/drain (S/D) electrodes of TFT and top

electrodes of MISM and MIM capacitor. In the structure of IGZO TFT, the minimization of IGZO area is key factor to reduce the leakage current. The area of patterned IGZO was 0.903 mm^2 and the radius of circular top electrodes for capacitors was 210 μm. The channel width/length (W/L) of TFT was 1000 μm /120 μm.

Electrical characteristics of devices were measured by HP-4145B semiconductor parameter analyzer and HP-4284A LCR meter in air at room temperature under dark condition. And time-of-flight secondary ion mass spectrometry (TOF-SIMS) and alpha step were measured for the ion profiles in the dielectric and the film thickness, respectively.

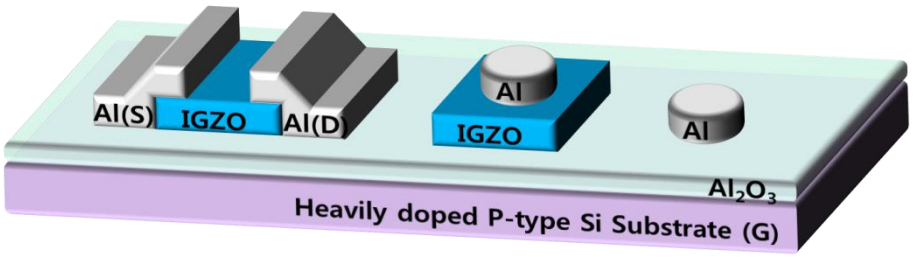


Figure 3.11 Schematic structures of IGZO TFT, MISM capacitor, and MIM capacitor on Al_2O_3 dielectric

3.3.2 Results and Discussion

Capacitance-frequency (C-V) and current density-voltage (J-V) characteristic of solution-processed Al_2O_3 dielectric in the MIM structure are in Figure 3.12. The capacitance of Al_2O_3 film was 90 nF/cm^2 and the dielectric constant was calculated to be 6.1. The leakage current density and breakdown voltage was 2.56×10^{-8} A/cm^2 at 1 MV/cm and 1.5 MV/cm, respectively. The leakage property can be further improved by patterning the gate electrode to block additional leakage paths. Transfer and output characteristics of the IGZO TFT are described in Figure 3.13 (a) and (b), respectively. TFT was operated in low voltage condition under 5 V, which was resulted from the high capacitance of Al_2O_3 dielectric. The extracted saturation field effect mobility (μsat), threshold voltage (V_{th}), subthreshold swing (S.S.), on/off ratio (I_{on}/I_{off}) of IGZO TFT were 32.5 cm^2/Vs, 1.60 V and 157 mV/dec, 1×10^6, respectively. The values of μsat and Vth were extracted by using the $I_{DS}^{1/2}$ vs. V_{GS} relationship and the all values were obtained at V_{DS} = 3 V.

To investigate the high mobility behavior of IGZO TFT, we measured the MISM capacitor. In Figure 3.14 (a), interestingly, unlike the MIM capacitor, which showed constant capacitance values over a range between 20 to 1 kHz, the MISM capacitor exhibited a dielectric dispersion behavior, the capacitance decreased as the frequency increased. Dielectric dispersion indicates that the mobile ions, which can dope the organic semiconductors [9], exist in the gate dielectric film. Considering the capacitance of MISM capacitor at 20 Hz, the mobility modified to 16 cm^2/V s. Even though the mobility was obtained using the capacitance at low frequency (20 Hz), it was still overestimated value because the transfer characteristics measured under the DC bias, but the capacitance measured under the AC bias.

Figure 3.14 (b) shows the hysteresis of IGZO TFT at V_{DS} = 0.1 V and TFT exhibited counter clockwise hysteresis behavior. In metal oxide TFTs with SiO_2, clockwise hysteresis loop was occurred due to the charge trapping at the semiconductor/dielectric interfaces as shown in Figure 3.14 (c). On the contrary,

counter clockwise hysteresis behaviors were found in the TFTs with dispersive dielectrics. It is attributed to the slow polarization of mobile ions in gate dielectrics and the charge injection from the gate dielectric [10].

TOF-SIMS results show the different ion profiles in Al_2O_3 film between MIM and MISM capacitor. We found that more H+ and OH- ions were detected in Al_2O_3 film in MISM compared to MIM as shown in Figure 3.15 (a) and (b). These ions made an EDL formation in Al_2O_3 layer when electric field applied [4], [5], [11]. Therefore, there were formed EDL in MISM capacitor, and EDL enhanced the capacitance as well as the on-current of TFTs, which indicated the high mobility and the high on/off ratio. Also, the increase of off-current and gate leakage can be explained by the increase of the hydroxyl groups in the dielectrics [12].

The mechanism of migration of H+ and OH- ions from semiconductor to dielectric layer and the stability of dielectric dispersion behavior IGZO TFT are under investigation. In dispersive dielectric for TFTs, the low frequency capacitance value of MIM capacitor has been typically used in most previous reports, but we propose that MISM capacitor measurement is more suitable for accuracy estimation of parameters due to the possibility of the additional EDL formation through the mobile ions migration.

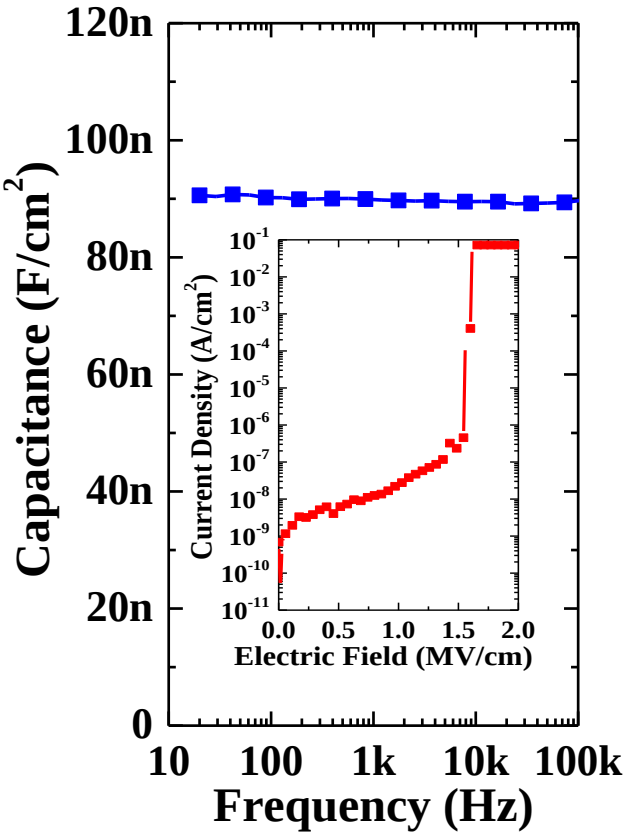


Figure 3.12 Capacitance-frequency (C-V) and current density-voltage (J-V) characteristic of solution-processed Al_2O_3 dielectric

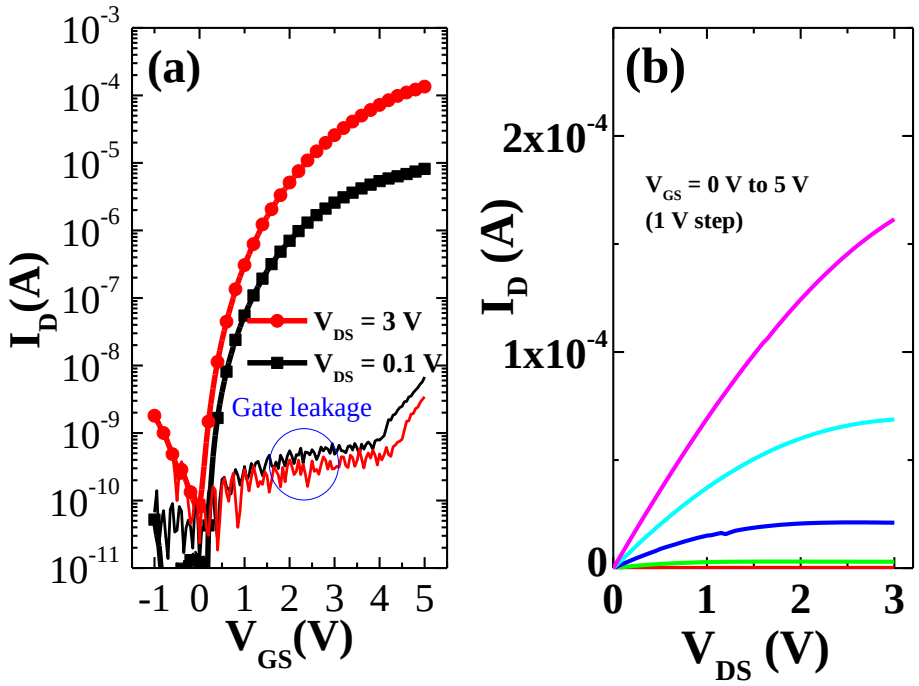


Figure 3.13 (a) Transfer and (b) output characteristics of the IGZO TFT on high-*k* Al_2O_3 dielectric layer.

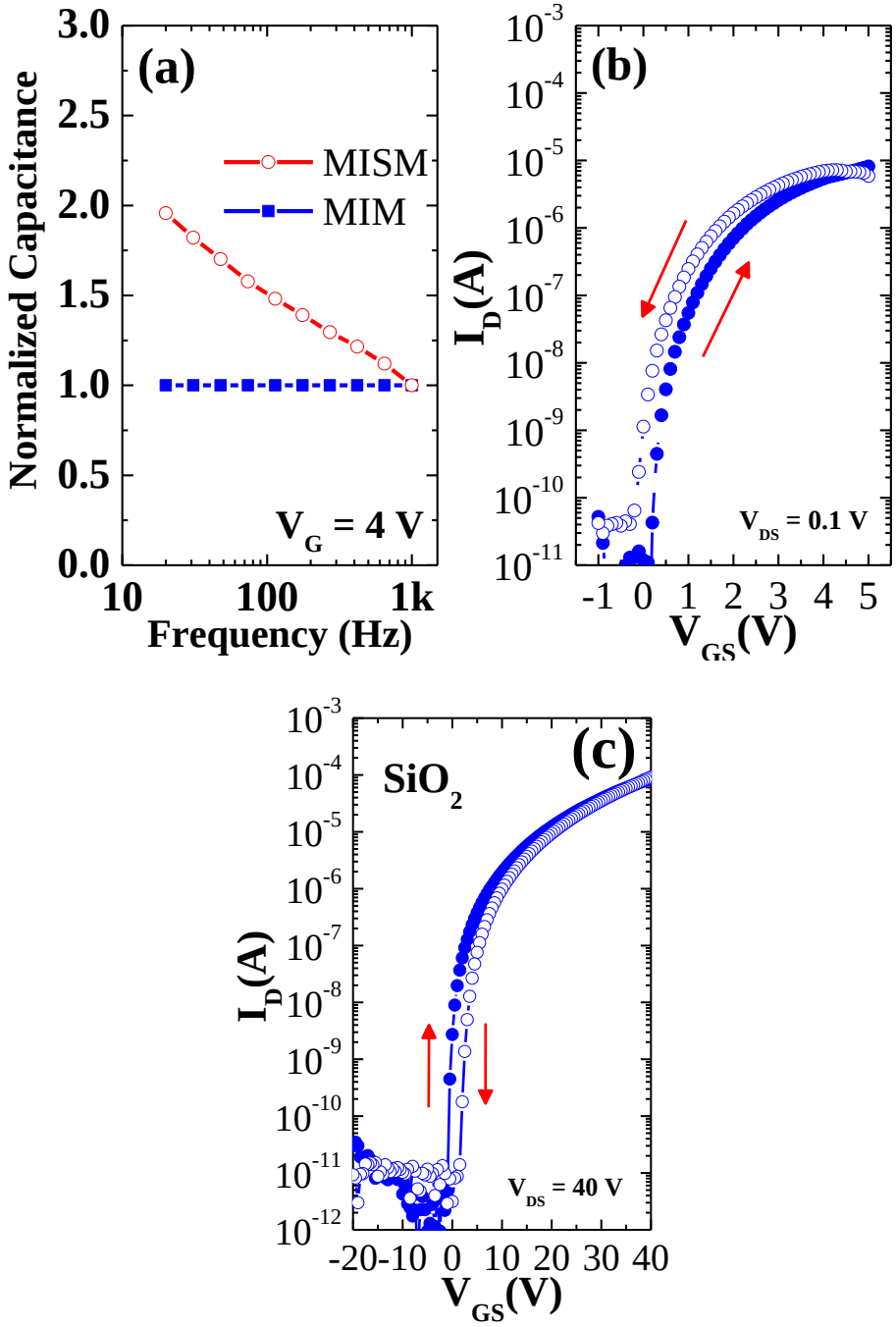


Figure 3.14 (a) Normalized capacitance of MISM and MIM capacitors. (b) Counter clockwise hysteresis of the IGZO TFT on Al_2O_3 layer at V_{DS} = 0.1 V. (c) Clockwise hysteresis of the IGZO TFT on SiO_2 layer at V_{DS} = 40 V.

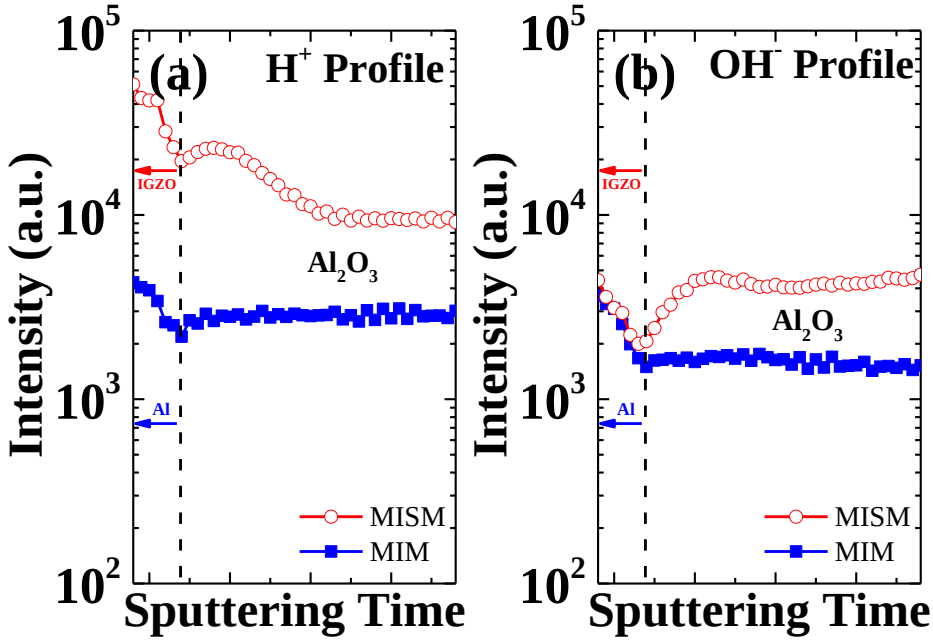


Figure 3.15 (a) H+ (b) OH- profiles of MISM and MIM capacitors obtained from TOF-SIMS measurement.

3.4 Low-Voltage Organic TFTs

3.4.1 Experimental

Bottom gate and top contact structure of p-type pentacene organic TFTs were fabricated with solution-processed high-*k* oxide gate insulators. Heavily boron doped p-type Si substrate was used for the gate electrode as well as the substrate. Pentacene active layer and Au source/drain electrodes were deposited by thermal evaporator continuously without vacuum breaking. The channel width (W) and length (L) of TFTs on Al_2O_3 dielectric were 1,000 μm and 45 μm, respectively. And the channel dimension of the TFTs on ZrO_2 was W/L = 1,000 μm/50 μm. Figure 3.16 shows the fabrication process and device structure of pentacene TFTs

For the low-voltage operation, two types of high-*k* oxide gate dielectrics were deposited onto the heavily doped p-type Si substrate by spin-coating. Precursor type ZrO_2 and Al_2O_3 solutions were prepared (Sigma-Aldrich) by 0.5 M zirconium chloride [ZrCl4] and zirconium isopropoxide isopropanol complex [$Zr(OCH(CH_3)_2) \cdot (CH_3)_2CHOH$] with a molar ratio of one and an aluminum nitrate nonahydrate [$Al(NO_3)_3 \cdot 9H_2O$] in 2-methoxyethanol [$CH_3OCH_2CH_2OH$], respectively. Both ZrO_2 and Al_2O_3 solution were spin-coated on heavily doped p-type Si substrates after the native oxide was removed and annealed at 500 and 300 ^oC, respectively. Several coatings were required to obtain desire thickness.

Electrical characteristics of devices were measured by HP-4145B semiconductor parameter analyzer and HP-4284A LCR meter in air at room temperature under dark condition. Also, to investigate a thickness of dielectric films and morphology of pentacene layer, field emission scanning electron microscope (FE-SEM, S-48000) and atomic force microscopy (AFM, XE-100) were performed.

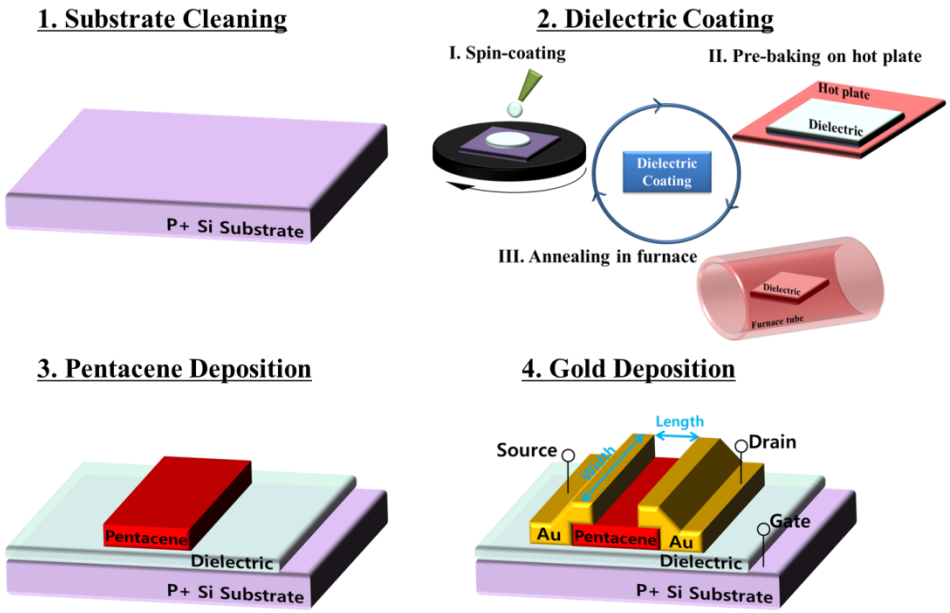


Figure 3.16 Fabrication process of low-voltage pentacene organic p-type TFTs with solution-processed high-*k* gate dielectrics.

3.4.2 Results and Discussion

Figure 3.17 shows the SEM images of solution-processed Al_2O_3 and ZrO_2 dielectrics. Thickness of Al_2O_3 film and ZrO2 film were 285 nm and 100 nm, respectively. Difference of thickness was originated from the multi-coating times and the molarity of solutions. Figure 3.18 shows capacitance-voltage characteristics and current density-voltage characteristics of both Al_2O_3 and ZrO_2 dielectrics from the MIM capacitors (p++ Si/high-*k*/Au). Capacitance measured at 100 kHz of Al_2O_3 and ZrO_2 films were 191 and 34.6 nF/cm^2, respectively, as shown in Figure 3.18 (a). Calculated dielectric constant of Al_2O_3 and ZrO_2 films were 11 and 22, respectively. Also, current density measured at -3 V of Al_2O_3 and ZrO_2 films were 10^{-6} A/cm^2 and 10^{-8} A/cm^2, respectively, as shown in Figure 3.18 (b). High capacitance of ZrO_2 film was attributed to the thin thickness and the high permittivity.

Figure 3.19 shows the XRD results of Al_2O_3 and ZrO_2 dielectrics. Al_2O_3 film shows the amorphous phase and ZrO_2 film shows the polycrystalline phase of mixture of monoclinic and tetragonal phase as mentioned in Chapter 2.3.1. Contact angle measurements were performed on the fabricated both high-*k* dielectric films.

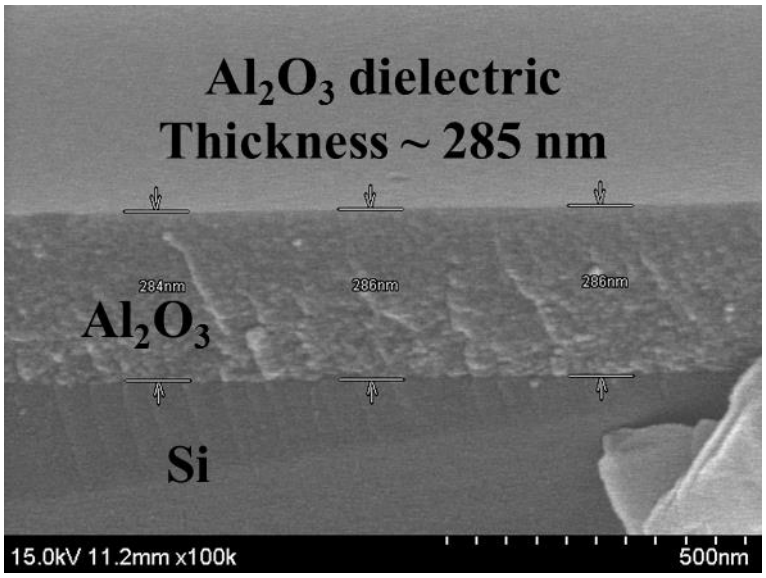
The contact angle of Al_2O_3 film was larger than that of ZrO film in both water and diiodomethane measurements as shown in Figure 3.20. A Surface energy can be converted from the contact angle by Owens-Wendt model. The surface energy of Al_2O_3 and ZrO_2 dielectric films were 28.48 and 34.74 mJ/m^2, respectively. It indicated that the Al_2O_3 dielectric film was more hydrophobic surface than ZrO_2 film. Pentacene growth is strongly influenced by surface free energy [13]. Hydrophobic property of dielectric layer is suitable for pentacene growth. The contact angle results and the parameters (dispersion term and polar term) of surface energy are summarized in Table 3.2.

Figure 3.21 shows the AFM images of the both Al_2O_3 and ZrO_2 dielectric films. Al_2O_3 dielectric film shows the very smooth surface properties such as peak-to-valley of 1.81 nm and rms roughness of 0.218 nm. On the contrary, ZrO_2 film has

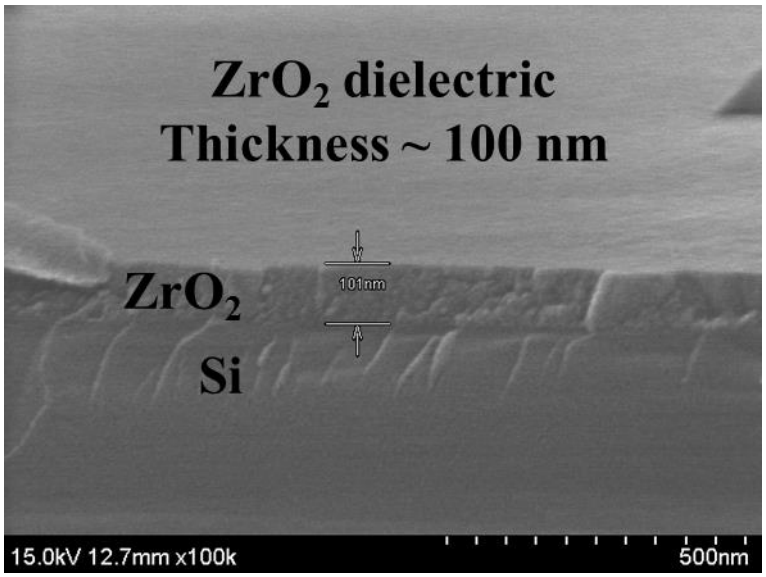
the peak-to-valley of 5.64 nm and rms roughness of 1.28 nm. In organic TFTs, surface property affects the semiconductor growth and morphology as well as the semiconductor/dielectric interface property [14].

Pentacene TFTs on Al_2O_3 and ZrO_2 gate dielectric were operated well under the low-voltage condition under 3 V due to the high capacitance of gate insulators, which induced more charges at the pentacene/dielectric interface, as shown in Figure 3.22 and 3.23, respectively. The mobility, Vth, S.S., and Ion/Ioff of TFT on Al_2O_3 insulator were > 4 cm^2/Vs, -0.416 V, 0.145 V/dec, and ~ 10^4, respectively. And the mobility, Vth, S.S., and Ion/Ioff of TFT on ZrO_2 insulator were > 0.09 cm^2/Vs, -0.239 V, 0.251 V/dec, and > 10^4, respectively. TFT on Al_2O_3 insulator exhibited the superior electrical behavior of higher mobility and smaller S.S. compared to TFT on ZrO_2 insulator. Interestingly, on-current of the pentacene TFT on the Al_2O_3 dielectric was at least 8 times higher than that of ZrO_2 dielectric TFT even though Al_2O_3 film has the low capacitance. Electrical parameters of the two TFTs are listed as Table 3.3 and parameters were extracted in saturation region using the capacitance at 100 kHz.

Figure 3.24 shows the XRD result of the pentacene films on the Al_2O_3 and ZrO_2 dielectrics. Sharp shape of the first order XRD peak (001) of pentacene film on the Al_2O_3 dielectric indicated that the good molecular ordered pentacene layers were grown. Besides, AFM analysis revealed that both pentacene layers were grown in dendritic shape, but grain size were different as shown in Figure 3.25. Small grains were formed in pentacene film on the ZrO_2 insulator as shown in Figure 3.25 (b). It indicated that the high density of grain boundary was existed in active layer. However, large grain pentacene film was grown on the Al_2O_3 dielectric as shown in Figure 3.25 (a). Large grain, which meant the low number of grain boundary, and highly ordered pentacene molecular properties were attributed to the smooth and the hydrophobic surface of Al_2O_3 film and those results accounted for the enhanced electrical characteristics [15].

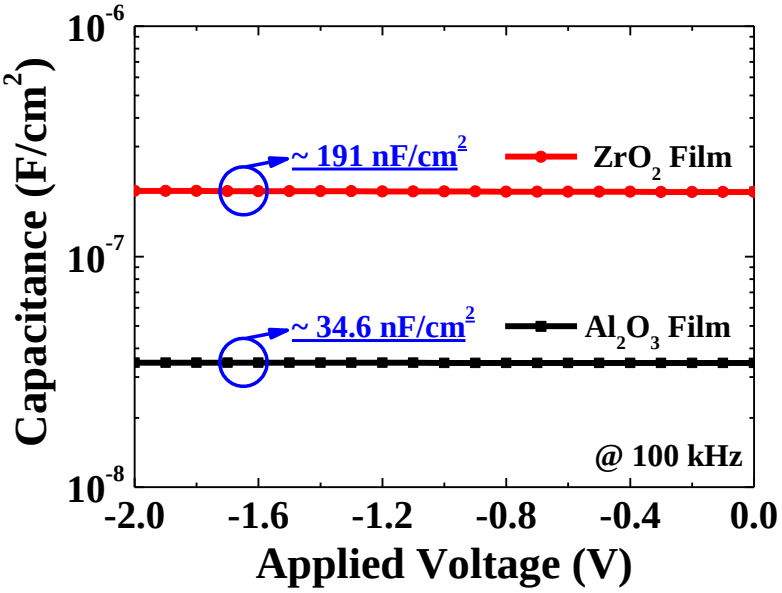


(a)

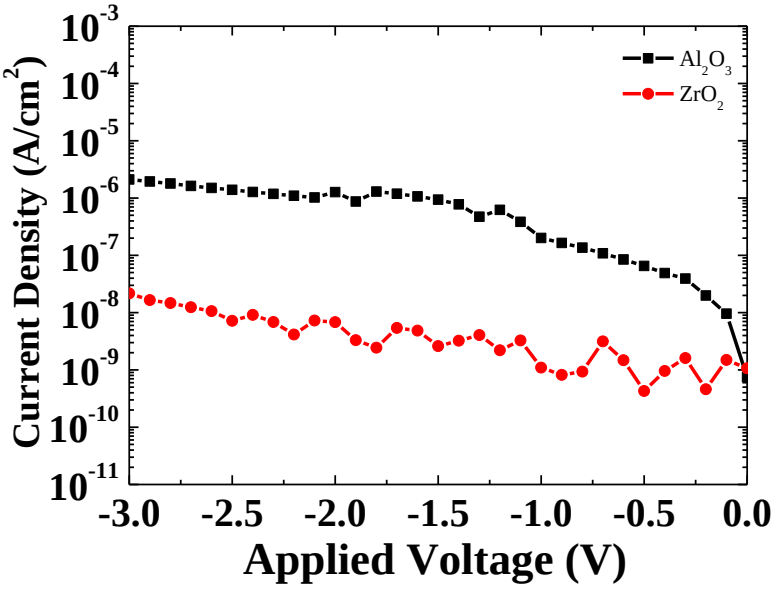


(b)

Figure 3.17 SEM image of solution-processed high-*k* dielectrics for pentacene organic TFTs: (a) Al_2O_3 dielectric and (b) ZrO_2 dielectric

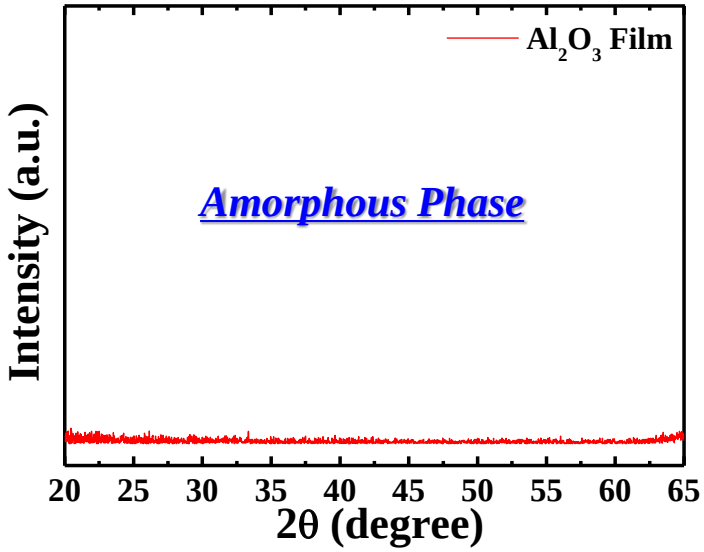


(a)

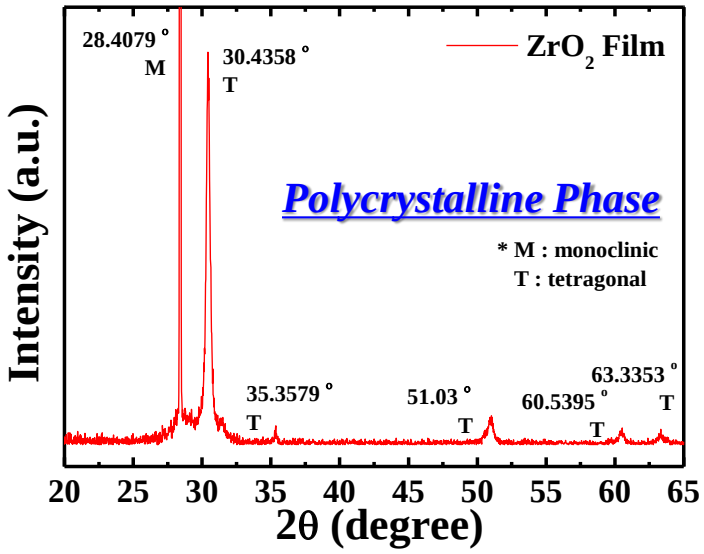


(b)

Figure 3.18 Electrical characteristics of solution-processed high-*k* Al_2O_3 and ZrO_2 MIM capacitors: (a) capacitance-voltage characteristics and (b) leakage current density-voltage characteristics

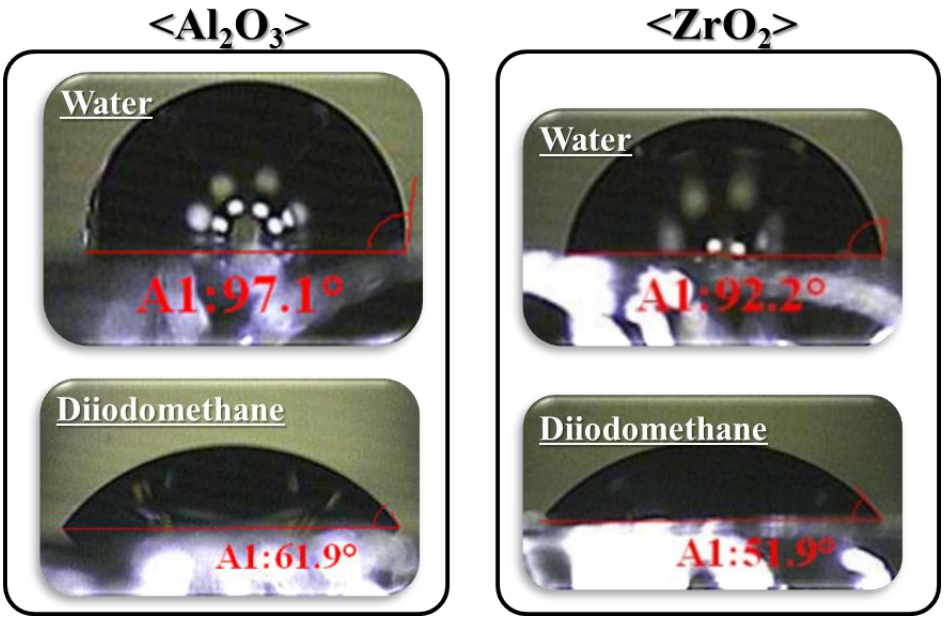


(a)



(b)

Figure 3.19 XRD results of solution-processed high-*k* dielectric for low-voltage pentacene organic TFTs: (a) amorphous phase Al_2O_3 and (b) polycrystalline phase ZrO_2

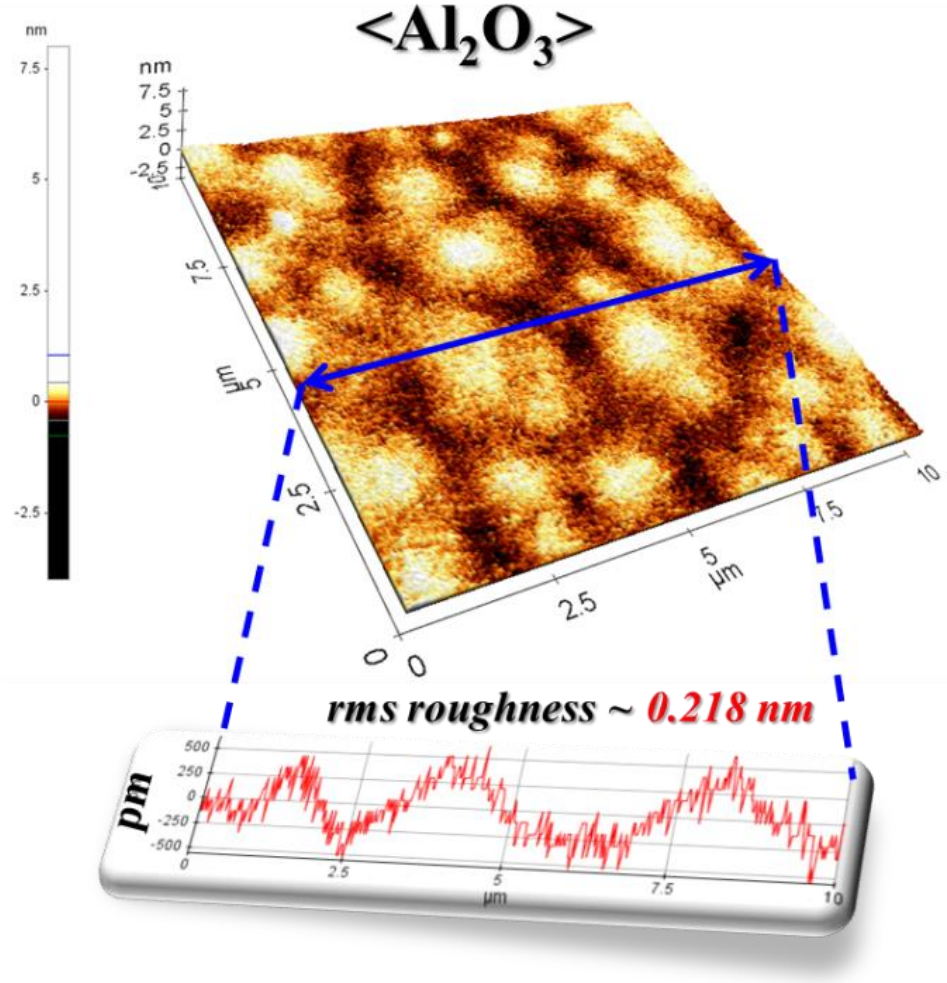


(a) (b)

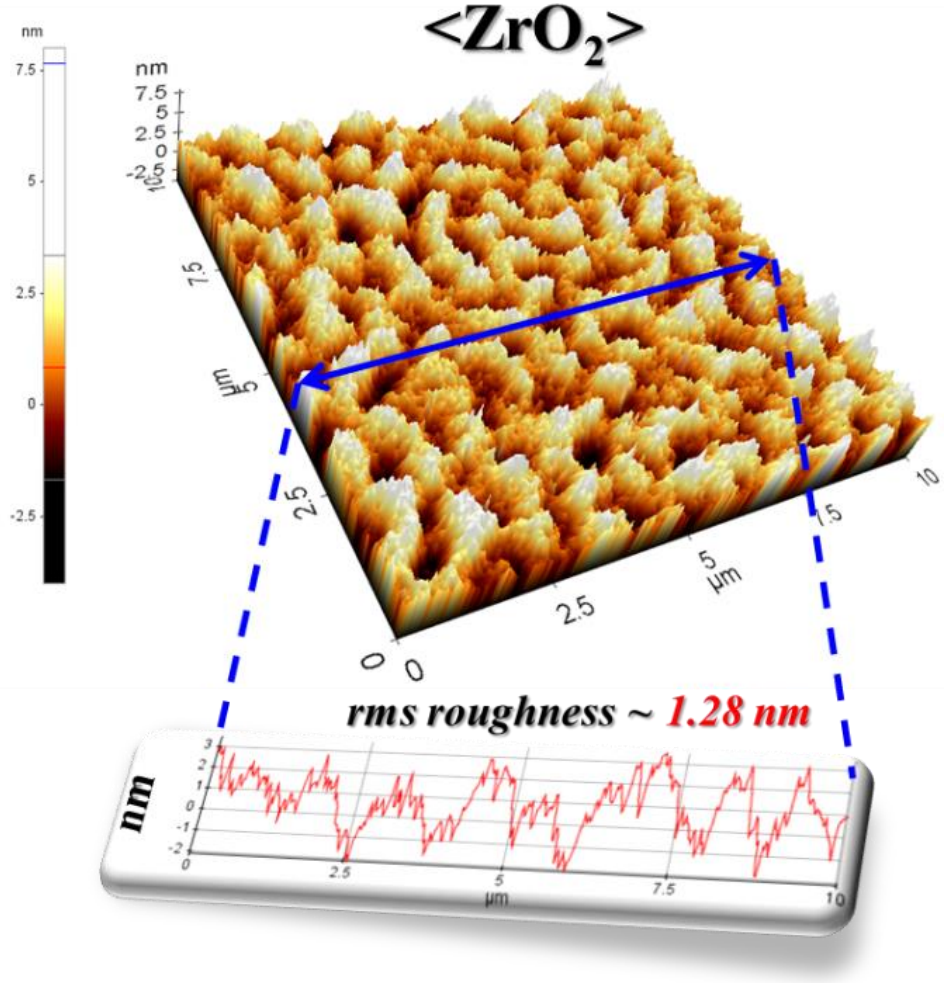
Figure 3.20 Images of contact angle measurements with water and diiodomethane solution: (a) Al_2O_3 film and (b) ZrO_2 film

Table 3.2 Results of contact angle measurements and parameters of surface energy.

Dielectric	Contact angle (deg)		Dispersion term [mJ/m^2]	Polar term [mJ/m^2]	Surface energy [mJ/m^2]
	Water	Diiodomethane			
Al_2O_3	97.1	62.1	27.39	1.10	28.48
ZrO_2	92.1	51.4	33.47	1.27	34.74

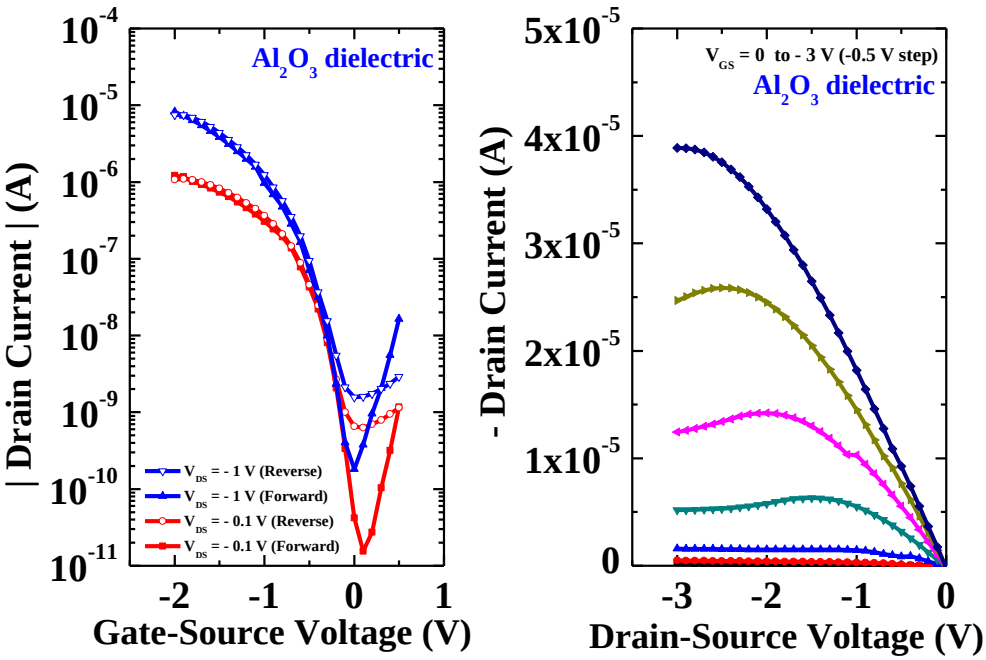

<Al2O3>
nm
7.5
5
2.5
0
-2.5
μm
rms roughness ~ 0.218 nm
pm
500
250
0
-250
-500

(a)



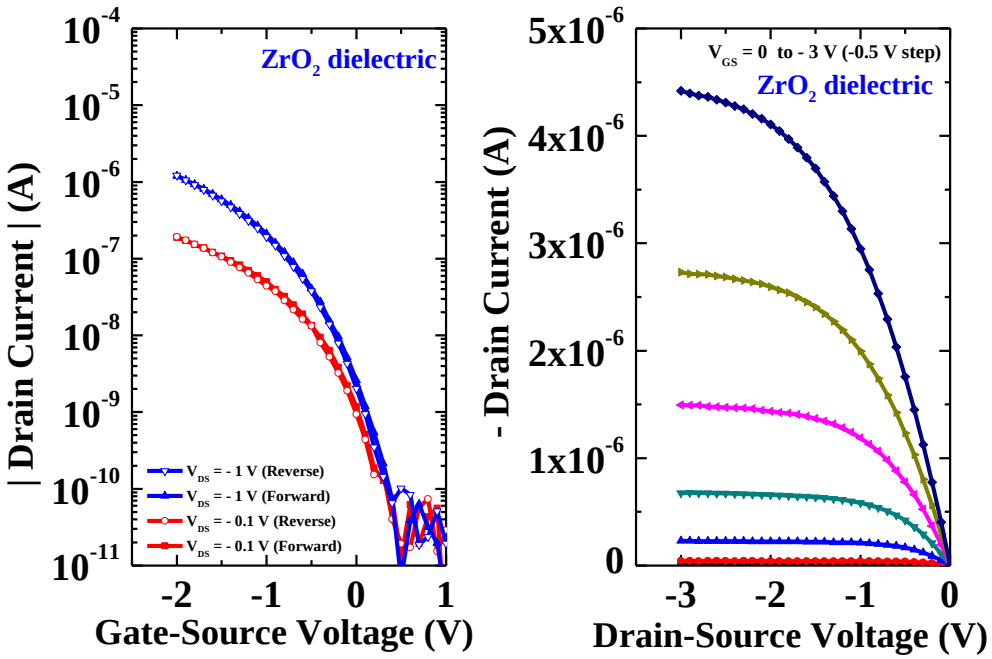
(b)

Figure 3.21 Surface morphology and roughness of solution-processed high-*k* dielectrics for low-voltage pentacene TFTs: (a) Al_2O_3 and (b) ZrO_2



(a) (b)

Figure 3.22 (a) Transfer characteristics and (b) output characteristics of low-voltage p-type pentacene organic TFT on solution-processed Al_2O_3 dielectric.



(a) (b)

Figure 3.23 (a) Transfer characteristics and (b) output characteristics of low-voltage p-type pentacene organic TFT on solution-processed ZrO_2 dielectric.

Table 3.3 Electrical parameters of low-voltage p-type pentacene organic TFTs on the solution-processed high-*k* dielectrics.

Dielectric	C [nF/cm^2]	Operating Voltage [V]	Mobility [cm^2/V·s]	Vth [V]	S.S. [mV/dec]	I_{on}/I_{off}
Al_2O_3	36.4	3	> 4	-0.416	145	~ 10^4
ZrO_2	191	3	0.09	-0.239	251	> 10^4

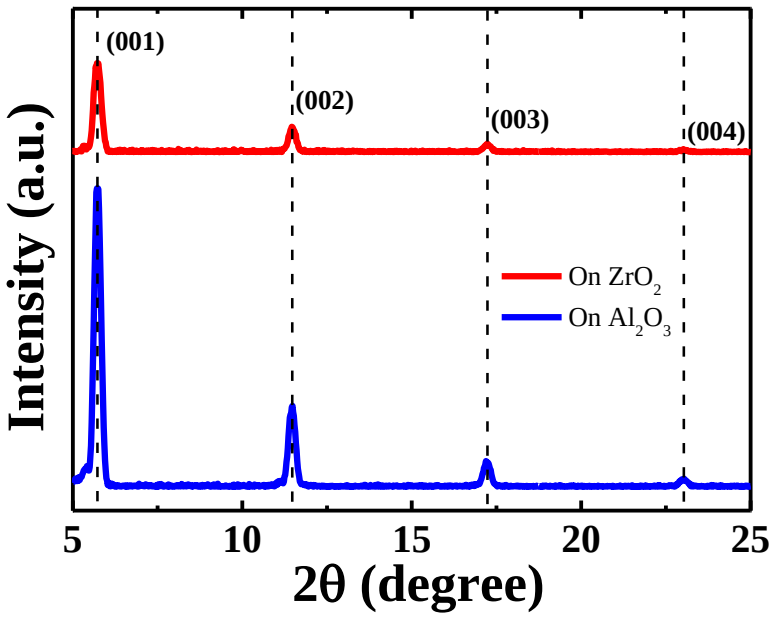
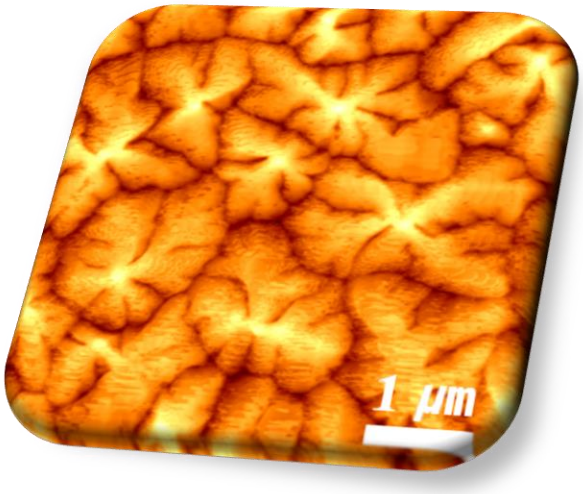
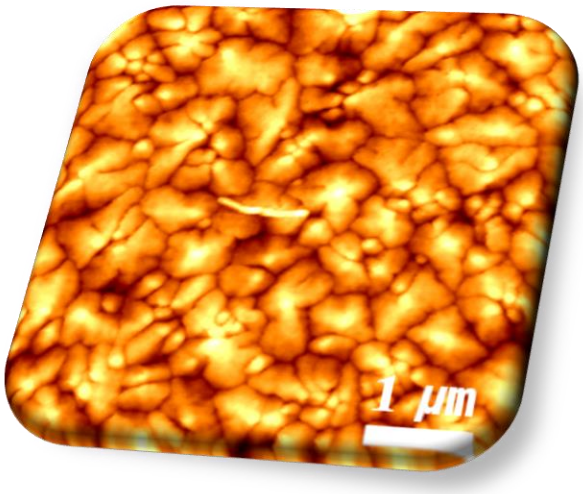


Figure 3.24 XRD result of the pentacene films on the Al_2O_3 and ZrO_2 dielectrics.



(a)



(b)

Figure 3.25 AFM images of the pentacene surface on the solution-processed high-*k* dielectrics: (a) Al_2O_3 and (b) ZrO_2

3.5 Summary

In conclusion, both high capacitance of gate dielectrics enabled oxide and organic TFTs to operate in low-voltage condition under the 5 V as well as enhancement of electrical characteristics. In particular, Al_2O_3 dielectric exhibited better TFT electrical behaviors such as high mobility and steep S.S. than ZrO_2 dielectrics.

High-performance IGZO TFTs on high-*k* Al_2O_3 dielectric were fabricated by solution-process and operated under low voltage condition. TFTs showed an enhanced mobility of 16 $cm^2/V{\cdot}s$. Comparing the MISM and MIM capacitors, Al_2O_3 film in MISM structure exhibited dielectric dispersion behavior. And dielectric dispersion and counter clockwise hysteresis were supported by high H+ and OH- ions in MISM structure. Hence, the enhanced high-performance TFT was originated from the EDL formation of Al_2O_3 dielectric.

Pentacene TFTs with solution processed high-*k* oxide gate dielectric using ZrO_2 and Al_2O_3 were fabricated and operated well in the low-voltage range. ZrO_2 dielectric OTFT shows the mobility of 0.09 $cm^2/V{\cdot}s$, but Al_2O_3 dielectric OTFT shows the high mobility of above 4 $cm^2/V{\cdot}s$. It was originated from the grain size of pentacene layer and AFM images revealed that large pentacene grains were grown on the Al_2O_3 film, thus Al_2O_3 dielectric TFT shows the much higher on-current.

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Chapter 4 Solution-Processed Organic/Inorganic Hybrid CMOS-type Inverter

4.1 Introduction

Complementary metal-oxide-semiconductor (CMOS)-type circuits using thin-film transistors (TFTs) have been extensively investigated due to their potential use in large area and flexible electronic systems. In comparison to logic circuits composed of unipolar TFTs, CMOS-type circuits have merits of low power consumption, high gain, high noise margin, and simple circuit design.

Over the last few decades, organic materials have been developed to both p- and n-type semiconductor materials. Organic CMOS-type inverters were demonstrated but there are some issues on the stability and the low mobility of n-channel materials. So, in many cases, logic circuits composed of unipolar p-type OTFTs have been demonstrated [1]-[5]. ZnO-based materials have been widely studied for the replacement of Si-based materials such as a-Si:H and poly-Si because

of their high mobility, optically high transparency related with the wide band gap. However, ZnO-based materials also have some issues on deficiency of p-type material, so that circuits have been demonstrated only n-channel TFTs [6], [7]. Figure 4.1 shows the catergorization of CMOS circuits including amipolar components.

Thus, organic/inorganic hybrid complementary structures, consist of organic and oxide for p- and n-channel materials, respectively, are required for the CMOS-type circuit implementations. Iechi et al. and Oh et al. proposed the hybrid CMOS-type inverter with pentacene p-channel and ZnO n-channel TFTs. However, until now, in most cases, the hybrid circuits were fabricated by high cost processes such as vacuum deposition and dry/wet etches including photolithography methods [8-11]. Also, for source/drain (S/D) electrodes, two kinds of metals such as Al for ZnO and Au for pentacene or Ti/Au bilayer were deposited for lowering charge injection barriers. Table 4.1 summarizes the previous reported organic/inorganic hybrid cmos-type circuits based on vacuum processes.

To avoid expensive those processes, solution-based processes have been extensively studied for electronic devices because of low manufacturing cost related with simple processes, large area compatibility, low temperature. Among solution-process methods, inkjet printing method has advantages of maskless patterning due to direct pattern definition, non-vacuum process, high throughput, large area manufacturing, and economical use of the inks.

In this chapter, I demonstrate the organic/inorganic hybrid CMOS-type inverter using 6,13-bis (triisopropyl-silylethynyl) pentacene (TIPS-PEN) and indium-

gallium-zinc-oxide (IGZO) for p-channel and n-channel semiconductor materials, respectively, and silver (Ag) S/D electrodes on SiO_2 dielectric as well as high-*k* Al_2O_3 dielectric. All the layers were simply inkjet-printed or spin-coated without the photolithography.

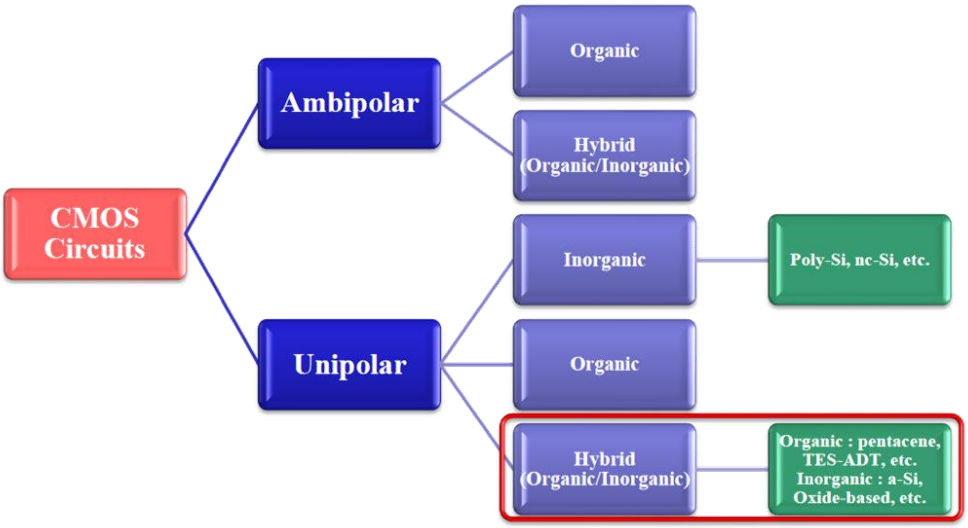
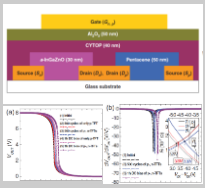
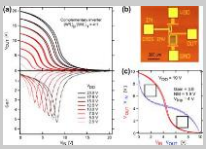
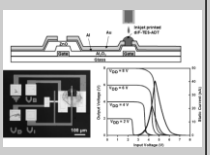
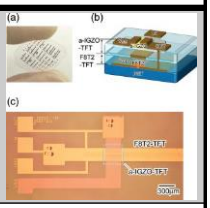


Figure 4.1 Various Types of CMOS circuits.

Table 4.1 Previous reported organic/inorganic hybrid CMOS circuits.

	J.B. Kim et al., *AIP Advances* 2, 0120134 (2012)	**M. Rockelé et al., *Organic Elec.* 12, 1909 (2011)**	**D.A. Mourey et al., *Organic Elec.* 14, 2411 (2013)**	**K. Nomura et al., *Appl. Phys. Lett.* 96, 263509 (2010)**
Structure				
Semiconductor Material	Pentacene (thermal evap.) a-IGZO (sputter)	Pentacene (thermal evap.) Metal oxide (spin-coating)	diF TES ADT (Inkjet-print) ZnO (PEALD)	F8T2 (inkjet-print) a-IGZO (PLD)
Circuits	Inverter	Inverter Ring oscillator	Inverter	Inverter
Performance	μ_p ~0.1 ± 0.01 cm^2/Vs μ_n ~5.0 ± 0.5 cm^2/Vs V_{DD} = 8 V Gain : 45 V/V	Inverter V_{DD} = 2.5 ~ 20 V Gain : 1.6 ~ 5.5 V/V Ring oscillator : 113 kHz, t_p = 0.73 μs, V_{DD} = 20 V	μ_p ~0.06 cm^2/Vs μ_n ~ 18 cm^2/Vs V_{DD} = 8 V Gain : 35 V/V	μ_p ~1.7×10^{-3} cm^2/Vs μ_n ~3.2 cm^2/Vs V_{DD} = 10, 20, 30 V Gain : 15, 40, 67 V/V

4.2 Hybrid CMOS on SiO_2 Dielectric

4.2.1 Structure and Fabrication Process

The hybrid CMOS-type inverter was fabricated on heavily doped p-type Si substrate by using solution processes and its structure is illustrated in Figure 4.2. The inverter is composed of bottom gate IGZO TFT with top contact and bottom gate TIPS-pentacene TFT with bottom contact. We used the heavily boron doped p-type Si substrate and thermally-grown SiO_2 with thickness of 200 nm for the gate and gate insulator, respectively.

Heavily doped p-type Si substrate was cleaned sequentially with acetone, isoprophyl alcohol (IPA) and deionized (DI) water in the ultra-sonicator at 40 ^{o}C for 20 min, respectively. Because IGZO solution was hydrophilic, the optimization of surface energy of SiO_2 layer was needed. Before inkjet printing of IGZO films, ultraviolet light/ozone (UVO) treatment was performed on the SiO_2 insulator for 5 min to lower the surface energy with cleaning the remained organic particles, so that the surface of SiO_2 layer was modified more hydrophilic.

For the inkjet printing of IGZO film as an active area, precursor type IGZO solution was prepared (Sigma-Aldrich) dissolving 0.3 M indium acetate, 0.1 M gallium nitride hydrate and 0.2 M zinc acetate dihydrate powders as precursors and 2-methoxyethanol (2ME) as a solvent. As a stabilizing agent, ethanolamine was used. The solution was stirred at 55 ^{o}C for 1 hour, then, aged at room temperature for 24 hours before injecting into a cartridge unit through hydrophilic filter. We used the piezoelectric type inkjet printer (DMP-2831, Dimatix corp.) and the 10 pL

cartridge (DMC-11601), which has 16 numbers of multi-nozzles and the diameter of each nozzle is about 21 μm. During inkjet printing of IGZO semiconductor, the substrate was kept at room temperature. We used 5 multi nozzles and the drop-spacing was adjusted to 25 μm. Drop-spacing is the distance between ink drops and main parameter for determination of the film quality such as egde wavyness [13]. Also, a velocity of IGZO ink drops from nozzle to surface of the substrate was about 4 m/s. After the printing of IGZO films, soft-baking was performed on the hot plate at 100 ^{o}C for 10 min to evaporate the solvent of IGZO. Then, to complete the chemical reaction of IGZO, the films were annealed at 500 ^{o}C for 1 hour in a furnace under atmospheric condition. With these optimized controlled jetting and wetting conditions including surface treatment, high-quality and uniform area was formed at the center of IGZO film on the SiO_2 layer, as shown Figure 4.3. In the structure of IGZO TFT, the minimization of IGZO area is key factor to reduce the leakage current.

Precursor type silver ink (TEC-IJ-010, InkTec corp.) was used for inkjet printing of S/D electrodes on the IGZO active layer and SiO_2 layer. During silver printing process, the substrate was kept at 60 ^{o}C. And the drop-spacing of each nozzle was adjusted to 25 μm. 6 nozzele with the drop velocity of 8.5 m/s were used for the silver inkjet-printing. To avoid unclearly defined IGZO area, which typically exists around the pattern edges, the channel was intentionally formed in the uniform region as shown in the magnified image of Figure 4.3. After the inkjet printing of silver electrodes, to evaporate the solvent of silver ink, substrates were sintered in a convection oven at 150 ^{o}C for 30 min. With the well-controlled silver inkjet-printing

conditions, highly conductive electrodes were deposited on the IGZO film and the effect of edge waviness was minimized. Thickness and sheet resistance of inkjet-printed silver electrodes were about 200 nm and 0.6 Ω/□, respectively.

For p-channel active layer, 1 wt% of TIPS-pentacene dissolved in 1,2-dichlorobenzene was drop-cast without surface treatment. To make high quality film related with molecular ordering, it is important to crystallize the film at slow speed [11]. To achieve highly ordered film, we used the 1,2-dichlorobenzene solvent because of its highly boiling point (~ 180 ^{o}C) and evaporating of solvent and crystallization of TIPS-pentacene were performed in air ambient at room temperature slowly for 1 hour. Considering the mobility difference between n-channel and p-channel TFTs, we designed p-channel and n-channel TFTs having different width/length (W/L) ratio in order to match charging and discharging current level during the inverter operation. The W/L of n-channel TFT was 220 μm / 100 μm and that of p-channel TFT was 5,000 μm / 55 μm. Figure 4.3 is optical images of the fabricated inverter. Electrical characteristics of devices and circuits were measured by Agilent 4155C semiconductor parameter analyzer in air at room temperature under dark condition.

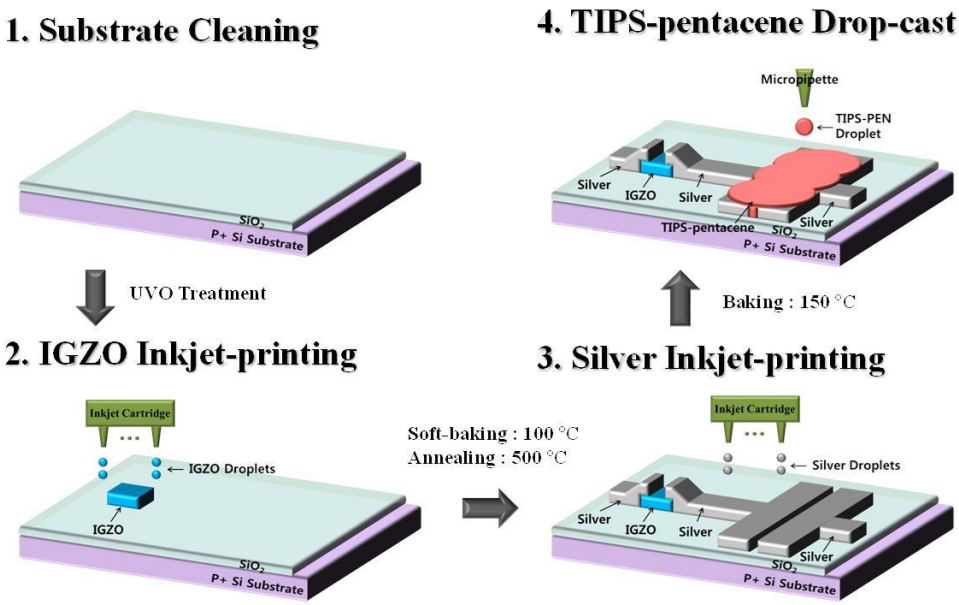


Figure 4.2 The fabrication processes of solution-processed hybrid CMOS-type inverter

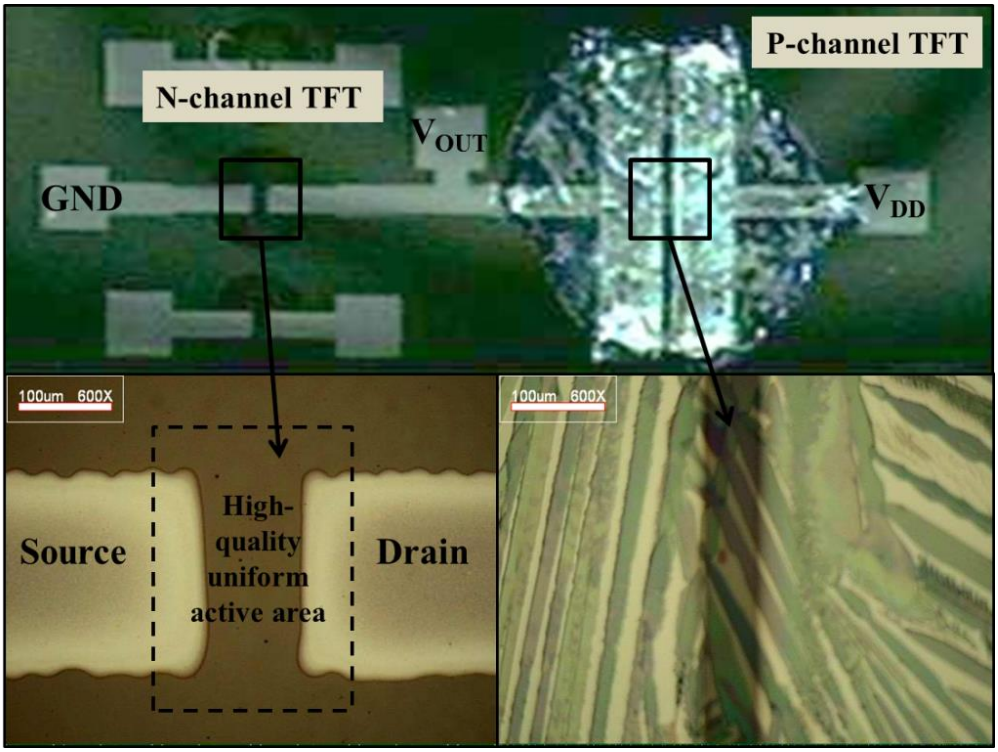


Figure 4.3 Optical images of fabricated inverter including high quality uniform region in n-channel TFT (bottom-left) and crystallized TIPS-PEN (bottom-right).

4.2.2 Electrical Characteristics

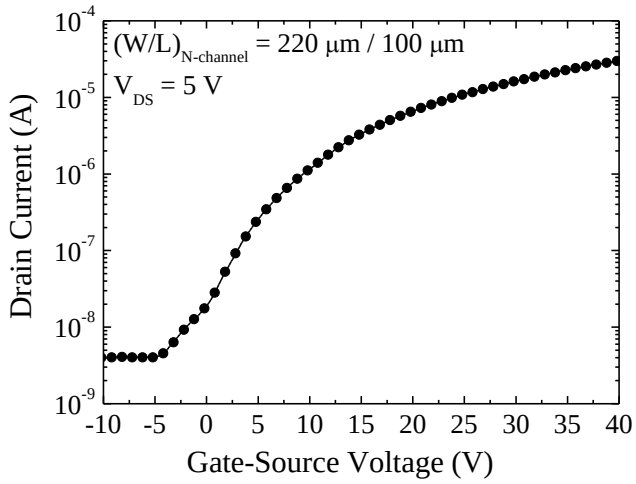
Figure 4.4 shows the electrical characteristics of the inkjet-printed IGZO TFT. The field effect mobility and threshold voltage of IGZO TFT were 4.55 cm^2/Vs and 7.18 V, respectively, and these values. The mobility is about 100 times higher than previously reported inkjet-printed IGZO TFTs [14]. High mobility was achieved due to the optimized inkjet-printing conditions such as jetting of IGZO from inkjet cartridge, wetting on the substrate, and substrate temperature during inkjet-printing process, and thus due to high-quality, uniform film formation. It is noted that channel was intentionally formed on the uniformly formed active region.

Figure 4.5 shows the I-V characteristics of the drop-cast TIPS-pentacene TFT. The field effect mobility and threshold voltage of p-channel TFT are 0.03 cm2/V•s and – 16.11 V, respectively. The on-current of p-channel TFT was 2 times lower than that of n-channel TFT even though inverter was designed to current matching. This non-current-matching will affect the behavior of inverter.

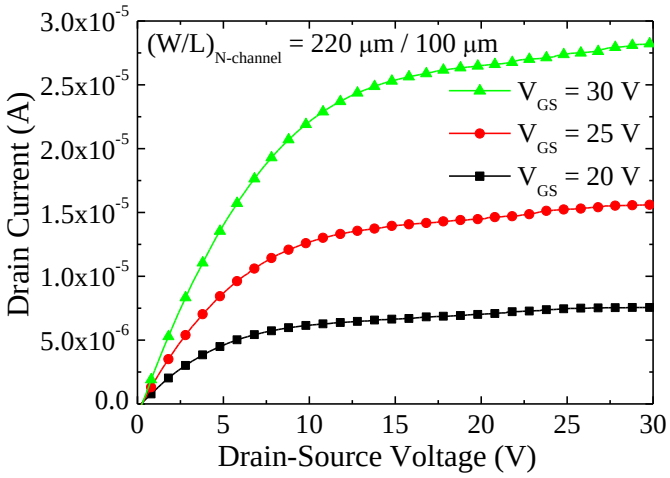
Figure 4.6 shows measured results of the fabricated inverter. Inverter behavior was observed only for $V_{DD} \geq 15$ V. It is believed that relatively high threshold voltages of both TFTs require high VDD for an appropriate operation of the fabricated inverter. Figure 4.6 (b) shows the gain of inverter calculated by dV_{OUT}/dV_{IN}.

Inverter gain increased with the increase of V_{DD} and the maximum gain – 22.23 V/V was achieved at V_{DD} = 40 V. This value is smaller than values of vacuum deposited hybrid inverters, but larger than that of p-type only organic inverters even though un-patterned gate electrode was used. In addition, the operating voltage was

small compared to organic inverters. It is noted that inverting transition of V_{OUT} did not take place around $V_{DD}/2$ for high V_{DD} values. It is speculated that the discharging current was increased due to the voltage stress effect during the measurement. Thus, the current discharging takes place before $V_{DD}/2$ as the V_{DD} increases. Further optimization of fabrication process and circuit design is expected to much improve the inverter performance

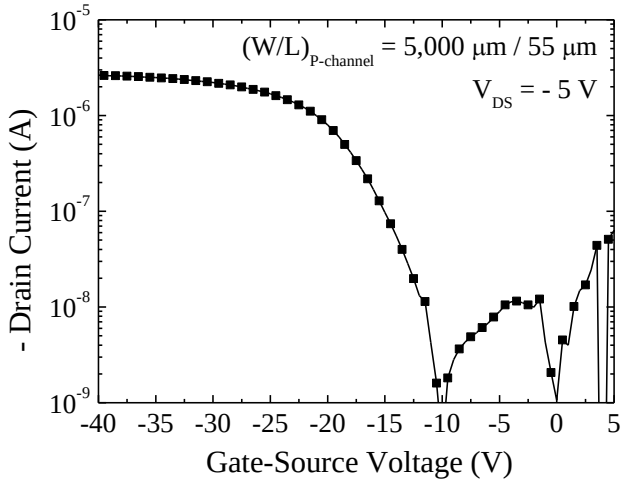


(a)

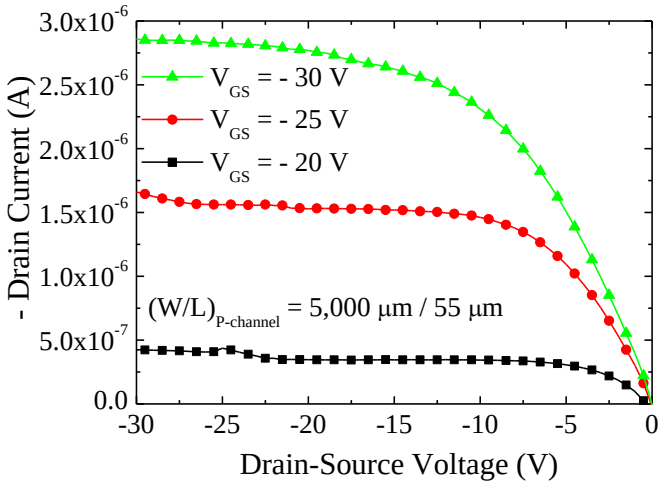


(b)

Figure 4.4 (a) The transfer characteristics of the inkjet-printed IGZO TFT at V_{DS} = 5 V. (b) The output characteristics of the IGZO TFT.

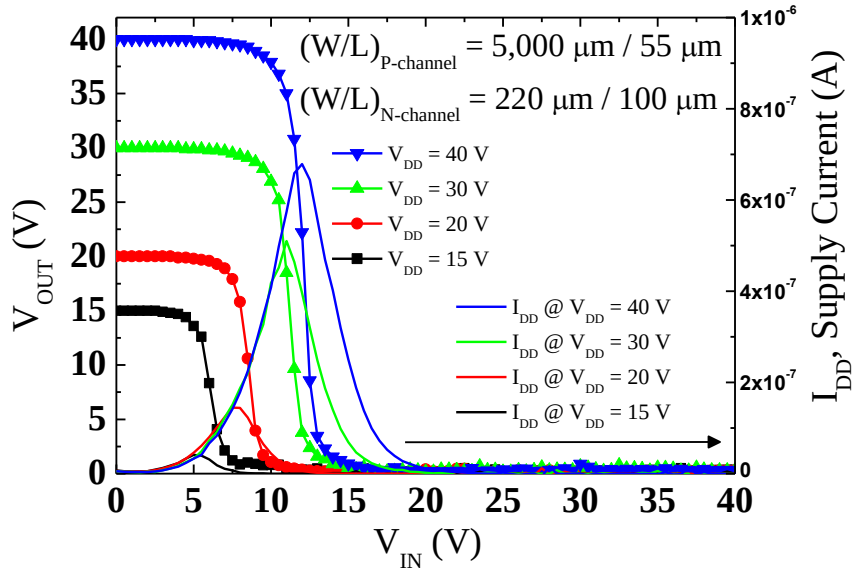


(a)

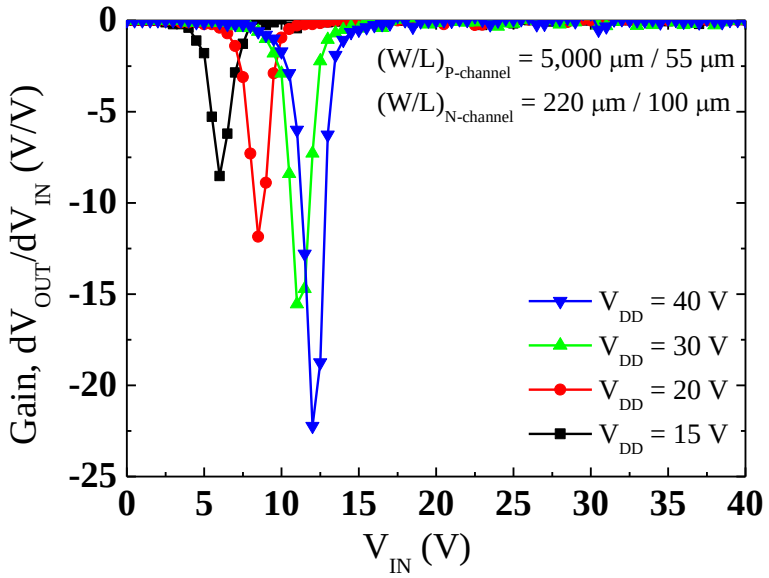


(b)

Figure 4.5 (a) The transfer characteristics of the fabricated TIPS-pentacene TFT at V_{DS} = - 5 V. (b) The output characteristics of the TIPS-pentacene TFT.



(a)



(b)

Figure 4.6 (a) The voltage transfer characteristics (b) gains of the fabricated hybrid CMOS-type inverter.

4.3 Low-Voltage Hybrid CMOS Inverter

4.3.1 Structure and Fabrication Process

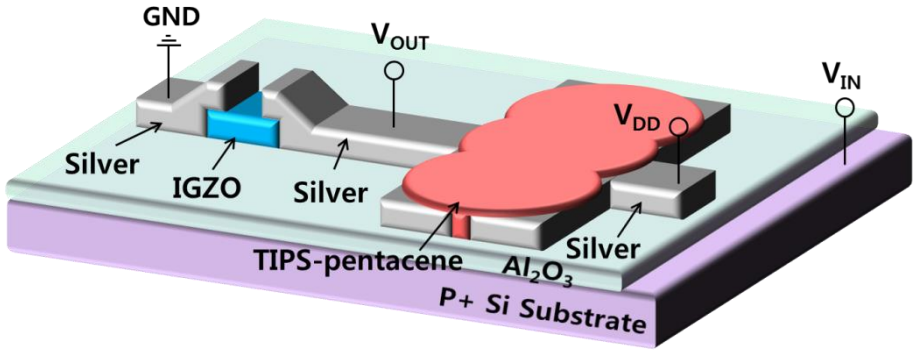
Oragnic/inorganic hybrid CMOS-type inverter composed of top-contact IGZO n-channel TFT and bottom-contact TIPS-PEN p-channel TFT was fabricated on an Al_2O_3 deposited heavily boron doped p-type Si substrate acting as a bottom-gate, as shown in Figure 4.7 (a). For a solution-processed high-*k* Al_2O_3 gate dielectric, precursor type solution was prepared (Sigma-Aldrich) dissolving an 0.5 M aluminum chloride in 2-methoxyethanol. To prevent abrupt evaporation of HCl gas in Al_2O_3 precursor, Al_2O_3 film was spin-coated on the heavily doped p-type Si substrate at 3000 r/min for 30 s in Ar_2 filled glove box and annealed carefully 500 ^oC for 4 h in air ambient furnace. Thermally annealed Al_2O_3 film showed the thickness of 60 nm.

After the preparation of high-*k* dielectrics, the precursor type 0.2 M IGZO n-type semiconductor solution was spin-coated on the dielectric and annealed at 400 ^oC in the furnace.

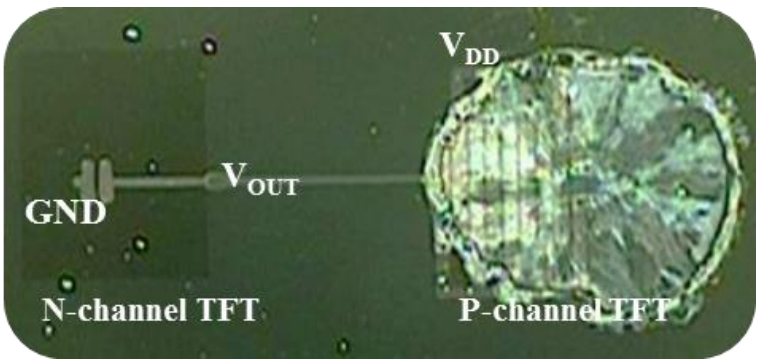
Nanoparticle silver (Ag) ink (Sigma-Aldrich) was used for S/D electrodes of both n- and p-channel TFT and directly patterned by inkjet printing. The substrate was kept at RT during Ag printing process, and then, annealed in a convection oven at 130 ^oC for 30 min. With the well-controlled silver inkjet-printing conditions, highly conductive electrodes were patterned on the substrate and the effect of edge waviness was minimized.

For p-channel active layer, 1 wt% of TIPS-PEN dissolved in toluene was printed in the channel region with a PS-brush treatment, which allows the hydrophobic and physicochemically stable properties of the surface [12], and then, crystallized in solvent-rich environment for 1 h. Considering the mobility difference between the two semiconductor materials, the inverter was designed p-channel and n-channel TFTs having different width/length (W/L) ratio in order to match charging and discharging current level during the inverter operation. The W/L of n-channel TFT was 400 μm / 200 μm and that of p-channel TFT was 5,000 μm / 100 μm.

Electrical characteristics of devices were measured by HP-4145B semiconductor parameter analyzer and HP-4284A LCR meter in air at room temperature under dark condition. Also, to investigate a thickness of dielectric films and morphology of pentacene layer, field emission scanning electron microscope (FE-SEM, S-48000) and atomic force microscopy (AFM, XE-100) were performed.



(a)



(b)

Figure 4.7 Organic/inorganic hybrid CMOS-type inverter. (a) Schematic structure. (b) Optical image of fabricated inverter including high quality uniform region in n-channel TFT (bottom-left) and crystallized TIPS-PEN (bottom-right).

4.3.2 Electrical Characteristics

Capacitance-frequency (C-*f*) and current density-voltage (J-V) characteristic of solution-processed Al_2O_3 dielectric are in Figure 4.8. For C-f and J-V measurements, Ag electrodes were patterned on Al_2O_3 spin-coated p++ Si substrate. The capacitance of Al_2O_3 film was 90 nF/cm^2 at 1 kHz by C-V measurement and the dielectric constant was calculated to be 6.1. The leakage current density was 100 nA/cm^2 at 5 V, which resulted from an additional leakage paths resulted from the use of un-patterned gate electrode.

Transfer characteristics of both IGZO and TIPS-PEN TFTs are described in Figure 4.9. Those TFTs operated in low voltage condition, which was resulted from the high capacitance of Al_2O_3 dielectric. However, the on-current of p-channel TFT was 2 times high than that of n-channel TFT due to the randomly crystallization of TIPS-PEN semiconductor even though inverter was designed to current matching.

Static voltage transfer characteristics of hybrid CMOS-type inverter were measured as shown in Figure 4.10 (a). Inverter behavior was observed from the small DC bias V_{DD} of 2 V. Figure 4.10 (b) shows the static gain of inverter calculated by dV_{OUT}/dV_{IN}. Inverter gain increased with the increase of V_{DD} and the maximum gain – 7.5 V/V was achieved at V_{DD} = 3 V. This value is smaller than values of vacuum deposited hybrid inverters, but larger than that of p-type only organic inverters considering the fabricated inverter used un-patterned gate electrode and operated in low voltage. Inverting transition of VOUT did not take place around $V_{DD}/2$ at given VDD values was indicated that the mismatch of V_{TH} and on-current levels. TIPS-PEN TFT exhibited the near zero V_{th} and the 2 times higher on-current

value, so that the switching threshold (Vinv) occurred after the $V_{DD}/2$ about 1.8 V. The Vinv can be expressed the following equation [14]:

$$, \quad V_{inv} = \frac{\sqrt{\beta_n / \beta_p} V_{TH,n} + (V_{DD} - V_{TH,p})}{1 + \sqrt{\beta_n / \beta_p}} \qquad (1)$$

where β is design factor defined as μCoxW/L and Cox is a capacitance of gate dielectric. Using the measured parameters, Vinv was calculated 1.6 V at VDD = 3 V, which value was well matched in the error range (extracted value = 1.8 V).

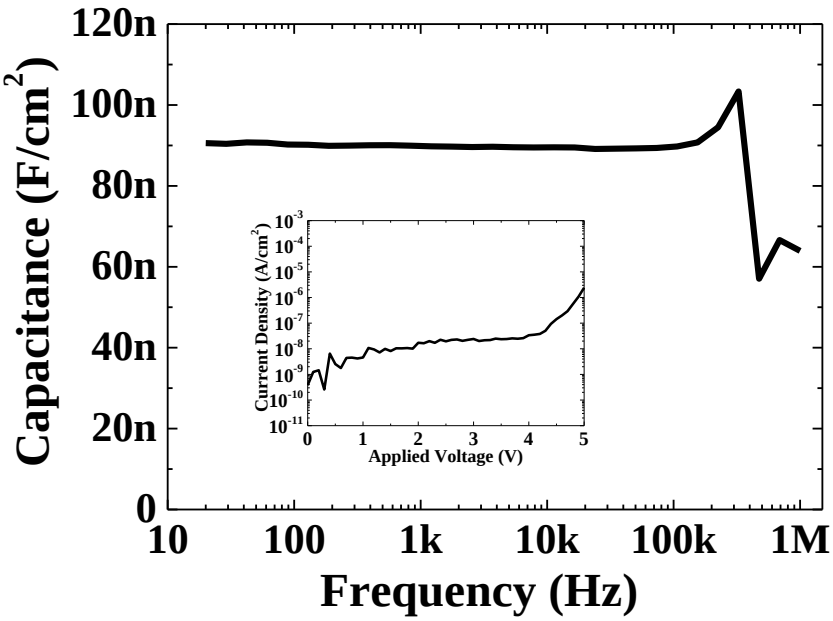


Figure 4.8 Capacitance-frequency (C-*f*) characteristic of solution-processed Al_2O_3 dielectric. (Inset) Current density-voltage (J-V) characteristic

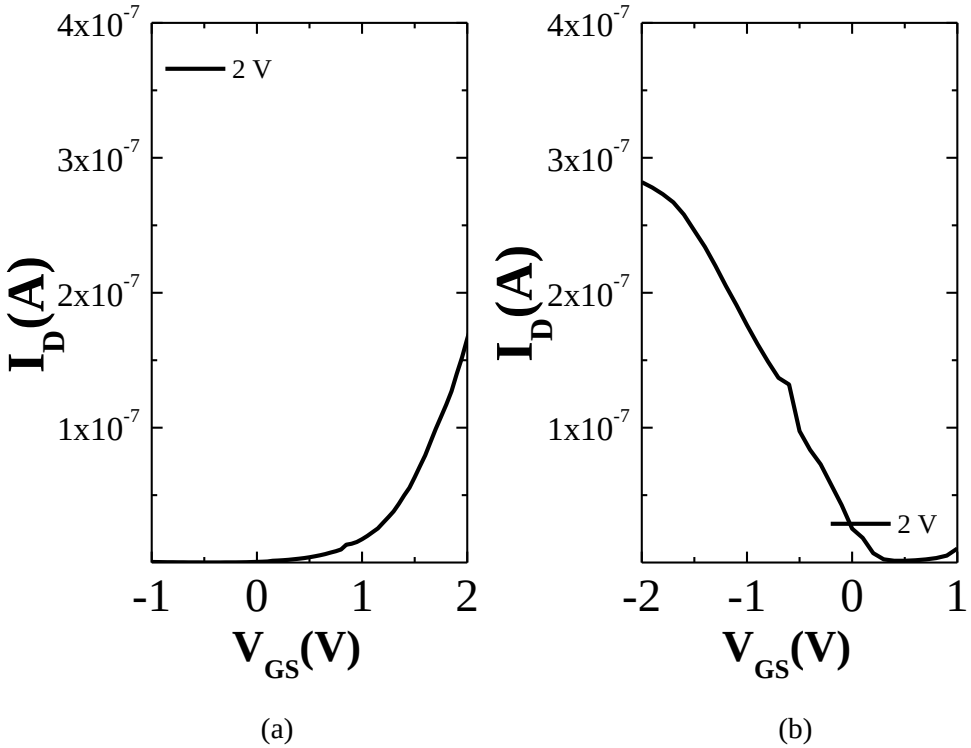
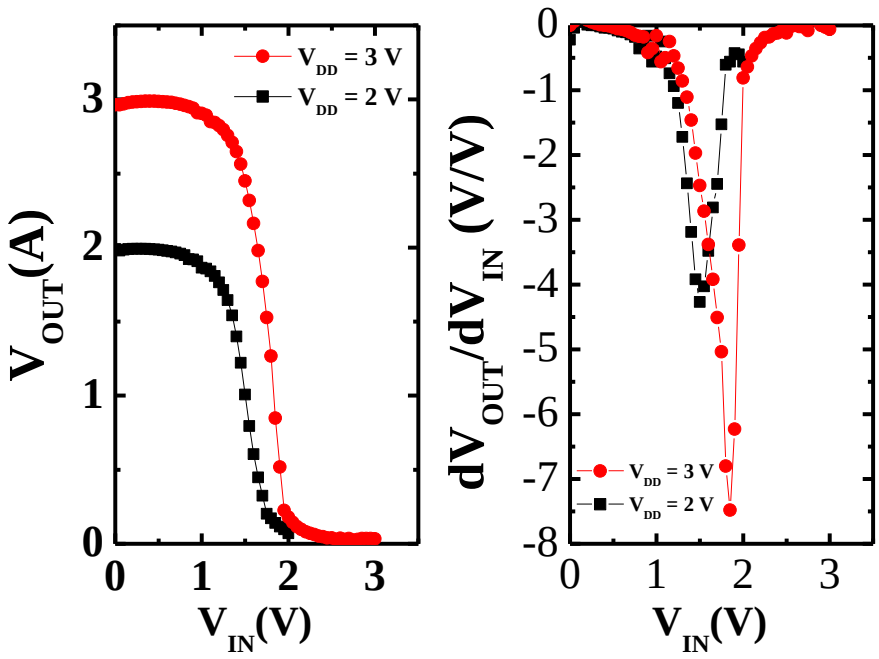


Figure 4.9 Transfer characteristics of inkjet-printed (a) IGZO and (b) TIPS-PEN TFT in the saturation regime.



(a) (b)

Figure 4.10 (a) The voltage transfer characteristics and (b) the gains of the fabricated hybrid CMOS-type inverter.

4.4 Summary

Organic/inorganic hybrid CMOS-type inverter was demonstrated using IGZO and TIPS-pentacene by solution-based processes, inkjet-printing and drop-cast. . N-channel IGZO TFT exhibited the high field effect carrier mobility (4.55 cm^2/Vs) due to the carefully optimized conditions. And p-channel TIPS-PEN TFT showed the mobility of 0.03 cm^2/Vs. Inverter shows the gain of – 22.23 V/V at V_{DD} = 40 V and was operated from V_{DD} = 15 V. CMOS inverter on high-*k* Al_2O_3 gate dielectric operated in low-voltage condition under 3 V and exhibited the maximum gain of -7.5 V/V at V_{DD} = 3 V. Our fabrication method was simple, fast, cost effective, furthermore, it was not required photolithography. To improve the inverter performance, further optimization of current-matching, enhancement of organic TFT property and reduction of parasitic capacitance by patterning the gate electrodes were required.

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Chapter 5 Conclusion

In this thesis, oxide and organic TFTs on high-*k* gate dielectrics were fabricated by solution-processes to study the effect of high capacitance dielectric layer on the electrical characteristics of TFTs such as mobility, Vth, S.S., and operating voltage. And the organic/inorganic hybrid CMOS-type inverter on high-k Al_2O_3 dielectric was demonstrated by all solution-process fabrication method.

The solution-processed IGZO TFTs, composed of inkjet-printed active channel layer and Ag S/D electrodes on SiO_2, were demonstrated with the various thermal annealing temperatures. XPS result indicated that IGZO films annealed at higher temperature attain more charge carriers due to thermally enhanced oxygen-vacancy formation processes. Thus, mobility and V_{th} were increased and negatively shifted as the temperature increased, respectively. Also, TFT with Ag S/D electrodes exhibited compatible electrical performance to the TFT with Al S/D electrodes. Optimizations of inkjet-printing and thermal annealing conditions were required to achieve high performance characteristics.

To investigate the effect of high capacitance gate dielectrics on the electrical characteristics of solution-processed TFTs, high-*k* Al_2O_3 and ZrO_2 gate dielectrics were fabricated by spin-coating method. Both high capacitance of gate dielectrics enabled oxide and organic TFTs to operate in low-voltage condition under the 5 V as well as enhancement of electrical characteristics. In particular, Al_2O_3 dielectric exhibited better TFT electrical behaviors such as high mobility and steep S.S. than ZrO_2 dielectrics in both organic and oxide TFTs. All solution-processed high-performance low-voltage IGZO TFTs were demonstrated and MISM capacitor measurement was proposed for accuracy estimation of parameters due to the possibility of the additional EDL formation through the mobile ions migration.

Finally, an organic/inorganic hybrid structure approach was proposed to achieve CMOS-type inverters. Demonstrated all solution-processed organic/inorganic hybrid CMOS-type inverter structure showed the improved electrical performance compared to previous reported inverters composed of only p-type TFTs. In addition, the hybrid CMOS-type inverter on the high-*k* dielectric exhibited the low-voltage operation as well as the high DC gain at the same bias compared to SiO_2 dielectrics.

The solution-processed low-voltage TFTs and organic/inorganic hybrid CMOS structure presented in this Ph.D dissertation can be applicable to promising future electronics including all inkjet-printed circuit and flexible display.

한글 초록

높은 이동도, 광학적인 높은 투명성, 용액 공정 가능성을 장점으로 갖는 산화물 반도체는 박막트랜지스터의 반도체 물질로서 광범위하게 연구되고 있다. 능동 행렬 액정표시장치와 능동 행렬 유기발광다이오드의 백플레인으로 사용될 수 있는 다양한 종류들의 산화물 반도체 기반의 소자들이 보고되고 있다. 산화물반도체 기반의 물질은 단순하고 저렴한 공정으로 기대되는 용액공정으로 제작 가능함에도 불구하고 값비싼 진공공정 장비를 이용해여 제작되고 있다. 최근 높은 전기용량을 갖는 절연체를 이용하여 박막소자들의 동작 전압을 낮추고자 하는 여러 노력들이 진행되고 있다. 높은 전기용량을 갖는 절연체를 사용하게 되면 낮은 전기용량을 갖는 절연체에 비해 같은 전압에서 더 많은 전하를 계면에 유도할 수 있으므로 낮은 전압조건에서 소자 및 회로의 동작이 가능할 것이다. 또한, 저전력 소비와 높은 전기적 성능을 달성할 수 있다.

본 연구의 목적은 저비용 용액 공정으로 제작된 고유전상수를 갖는 절연체를 이용하여 낮은 전압에서 작동하는 고성능 유기 및 무기 박막트랜지스터를 제작함과 동시에 이를 상보형 금속 산화 반도체 회로에 응용하는 것이다.

첫 번째로 indium−gallium−zinc−oxide (IGZO) 반도체 층과 Ag 소스/드레인 전극을 용액 공정의 하나인 잉크젯 프린팅 공정으로 제작하는 연구를 했다. 제작된 IGZO 박막트랜지스터는 400 °C 의 온도에서 2 cm^2/Vs 이상의 높은 이동도를 나타내었다. 고성능의 전기적 특성을 갖는 박막트랜지스터 제작을 위해서는 잉크젯 프린팅 및 열처리의 조건 최적화가 요구된다.

두 번째로 낮은 전압에서 구동하는 박막트랜지스터 연구를 위해 고유전상수를 갖는 Al_2O_3 및 ZrO_2 게이트 절연체를 스핀 코팅을 이용하여 제작했다. 높은 전기용량의 두 절연체를 이용하여 유기 박막트랜지스터 및 산화물 박막트랜지스터를 5 V 이하의 낮은 전압에서 구동할 수 있게 하였다. 특히, Al_2O_3 절연체는 비정실 상태의 특성을 나타냈으며 ZrO_2 절연체 위에 형성된 유기물 및 산화물 반도체 소자 대비 높은 전기적 특성을 나타내었다. 그리고 전 용액 공정으로 제작된 낮은 전압에서 작동하는 고성능 IGZO 박막트랜지스터를 제작함과 동시에 소자의 전기적 파라미터의 정확한 추출을 위해 MISM 캐패시터를 이용한 측정 방법을 제안하였다.

마지막으로 상보형 금속 산화 반도체 인버터 제작을 위해 유/무기 물질을 복합하여 활용하는 구조를 제안하였다. 제작된 복합 인버터는 기존에 보고된 유기 물질만을 이용한 단일 반도체 인버터보다 우수한 성능을 나타내었다. 또한, 고유전상수를 갖는

절연막의 복합 인버터에 미치는 영향을 연구하였고 인버터의 특성이 향상되는 결과를 도출하였다.

주요어: 박막트랜지스터, IGZO, 산화물 반도체, 고유전상수 절연체, 상보형 금속 산화 반도체, 인버터, 용액 공정, 잉크젯 프린팅, 유기물 반도체

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